GLF1100

Nano-Current Consumed, I_QSmart™ Load Switch

Product Specification

DESCRIPTION

The GLF1100 is an ultra-efficiency, 2 A rated, Load Switch with integrated slew rate control. The best in class efficiency makes it an ideal chose for use in IoT, mobile, and wearable electronics.

The GLF1100 features ultra-efficient I_QSmart™ technology that supports the lowest quiescent current (I_Q) and shutdown current (I_{SD}) in the industry. Low I_Q and I_{SD} solutions help designers to reduce parasitic leakage current, improve system efficiency, and increase battery lifetime.

The GLF1100 integrated slew rate control can also enhance system reliability by mitigating bus voltage swings during switching events. Where uncontrolled switches can generate high inrush currents that result in voltage droop and/or bus reset events, the GLF slew rate control specifically limits inrush currents during turn-on to minimize voltage droop.

GLF1100 Load Switch devices support an industry leading wide input voltage range and helps to improve operating life and system robustness. Furthermore, one device can be used in multiple voltage rail applications which helps to simplify inventory management and reduce operating cost.

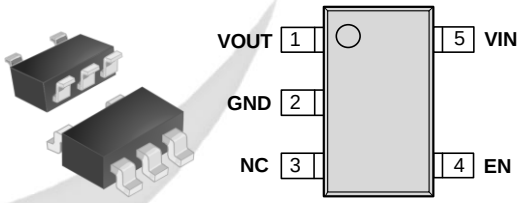
FEATURES

- Wide Input Range: 1.1 V to 5.5 V
  6 V abs max
- R_{ON} : 82 mΩ Typ @ 5.5 V_{IN}
- I_{OUT} Max: 2 A
- Ultra-Low I_Q: 10 nA Typ @ 5.5 V_{IN}
- Ultra-Low I_{SD}: 25 nA Typ @ 5.5 V_{IN}
- Controlled Rise Time: 2.2 ms at 3.3 V_{IN}
- Internal EN Pull-Down Resistor
- Integrated Output Discharge Switch
- Wide Operating Temperature Range:
  -40 °C ~ 85 °C
- HBM: 6 kV, CDM: 2 kV

APPLICATIONS

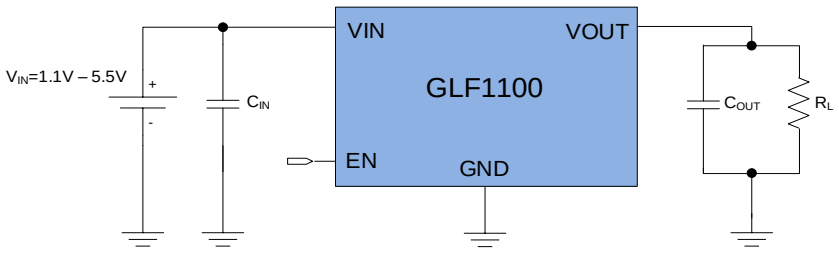
- Telecommunication Module
- Low Power Subsystem
- Mobile Devices

PACKAGE



SOT23-5

APPLICATION DIAGRAM



ALTERNATE DEVICE OPTIONS

Part Number	Top Mark	R_{ON} (Typ) at 5.5 V	Output Discharge	EN Activity
GLF1100-T1G7	CD	82 mΩ	85 Ω	High

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FUNCTIONAL BLOCK DIAGRAM

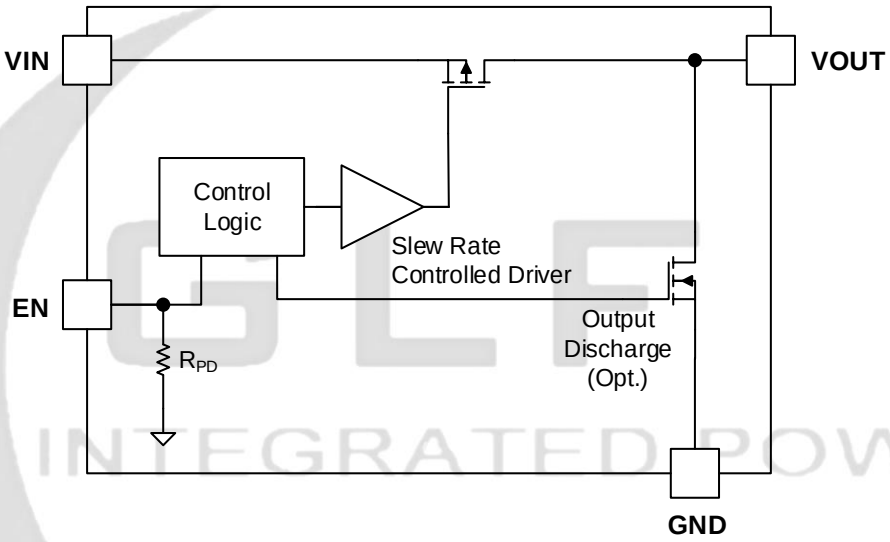


Figure 1. Functional Block Diagram

PIN CONFIGURATION

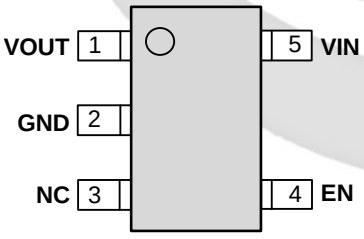


Figure 2. SOT23-5L

PIN DEFINITION

Pin #	Name	Description
1	V_{OUT}	Switch Output
2	GND	Ground
3	NC	No connection
4	EN	Enable to control the switch
5	V_{IN}	Switch Input. Supply Voltage for IC

ABSOLUTE MAXIMUM RATINGS

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions; extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{IN}	V_{IN}, V_{OUT}, V_{EN} to GND		-0.3	6	V
I_{OUT}	Maximum Continuous Switch Current			2	A
P_D	Power Dissipation at T_A = 25 °C			1.0	W
T_{STG}	Storage Junction Temperature		-65	150	°C
T_A	Operating Temperature Range		-40	85	°C
θ_{JC}	Thermal Resistance, Junction to Case			90	°C/W
θ_{JA}	Thermal Resistance, Junction to Ambient			180	°C/W
ESD	Electrostatic Discharge Capability	Human Body Model, JESD22-A114	6		kV
		Charged Device Model, JESD22-C101	2		

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Max.	Unit
V_{IN}	Supply Voltage	1.1	5.5	V
T_A	Ambient Operating Temperature	-40	+85	°C

ELECTRICAL CHARACTERISTICS

Values are at V_{IN} = 3.3 V and T_A = 25 °C unless otherwise noted.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Units
Basic Operation							
V_{IN}	Supply Voltage			1.1		5.5	V
I_Q	Quiescent Current (1)	EN = Enable, I_{OUT}=0 mA, V_{IN} = V_{EN} =5.5V			5		nA
		EN=Enable, I_{OUT}=0 mA, V_{IN}=V_{EN}=5.5V, Ta=85°C (4)			10		
		EN=Enable, I_{OUT}=0 mA, V_{IN}=V_{EN}=5.5V, Ta=105°C (4)			35		
I_{SD}	Shut Down Current	EN = Disable, I_{OUT}=0 mA, V_{IN}=1.1 V			3		nA
		EN = Disable, I_{OUT}=0 mA, V_{IN}=1.8 V			4		
		EN = Disable, I_{OUT}=0 mA, V_{IN}=3.3 V			6		
		EN = Disable, I_{OUT}=0 mA, V_{IN}=4.5 V			10		
		EN = Disable, I_{OUT}=0 mA, V_{IN}=5.5 V			25		
		EN = Disable, I_{OUT}=0 mA, V_{IN}=5.5 V, Ta=85 °C (4)			0.68		uA
R_{ON}	On-Resistance	V_{IN}=5.5 V, I_{OUT}= 500 mA	Ta=25 °C		82		mΩ
			Ta=85 °C (4)		98		
		V_{IN}=3.3 V, I_{OUT}= 500 mA	Ta=25 °C		88		
			Ta=85 °C (4)		104		
		V_{IN}=1.8 V, I_{OUT}= 300 mA	Ta=25 °C		104		
		V_{IN}=1.1 V, I_{OUT}= 100 mA	Ta=25 °C		161		
R_{DSC}	Output Discharge Resistance	E_N=Low , I_{FORCE}= 10 mA			85		Ω
V_{IH}	EN Input Logic High Voltage	V_{IN}=1.1 V – 1.8 V		0.9			V
		V_{IN}=1.8 V - 5.5 V		1.2			V
V_{IL}	EN Input Logic Low Voltage	V_{IN}=1.1 V – 1.8 V				0.3	V
		V_{IN}=1.8 V - 5.5 V				0.4	V
R_{EN}	EN pull down resistance	Internal Resistance			10		MΩ
I_{EN}	EN Current	E_N=5.5 V			0.5	1.0	μA
Switching Characteristics (2, 3, 4)							
t_{dON}	Turn-On Delay	R_L=150 Ω, C_{OUT}=0.1 μF			1.5		ms
t_R	V_{OUT} Rise Time				2.2		
t_{dON}	Turn-On Delay	R_L=500 Ω, C_{OUT}=0.1 μF			1.3		
t_R	V_{OUT} Rise Time				2.0		
t_{dOFF}	Turn-Off Delay	R_L=150 Ω, C_{OUT}=0.1 μF			1.2		us
t_F	V_{OUT} Fall Time				14		
t_{dOFF}	Turn-Off Delay	R_L=500 Ω, C_{OUT}=0.1 μF			1.2		
t_F	V_{OUT} Fall Time				17		

Notes:
1. I_Q does NOT include Enable pull down current through the pull down resistor R_{PD}.
2. t_{ON} = t_{dON} + t_R, t_{OFF} = t_{dOFF} + t_F
3. Output discharge path is enabled during off.
4. By design; characterized, not production tested

TIMING DIAGRAM

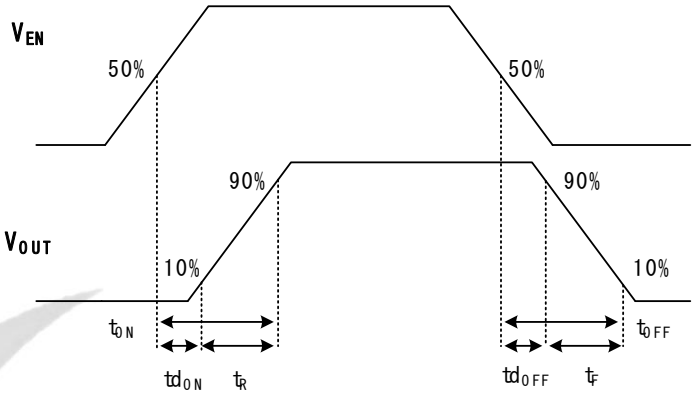


Figure 3. Timing Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

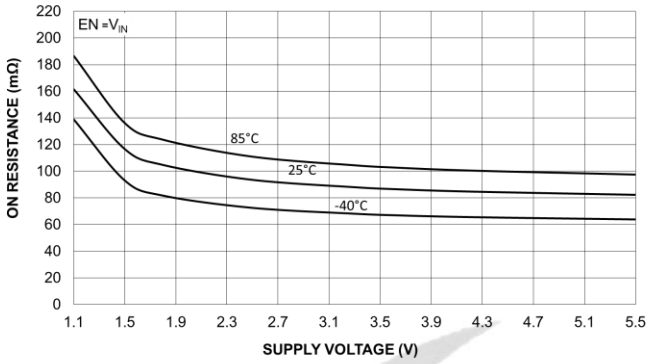


Figure 4. On-Resistance vs. Supply Voltage

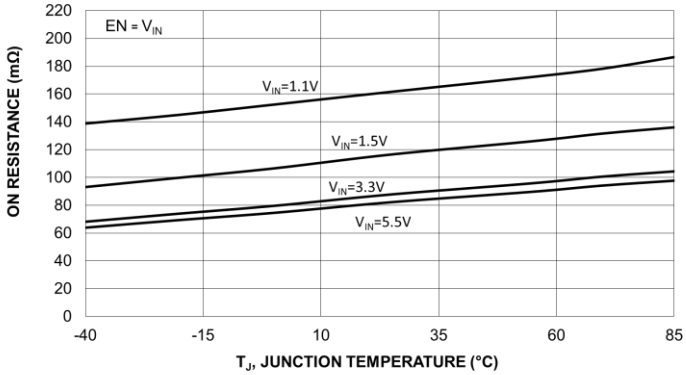


Figure 5. On-Resistance vs. Temperature

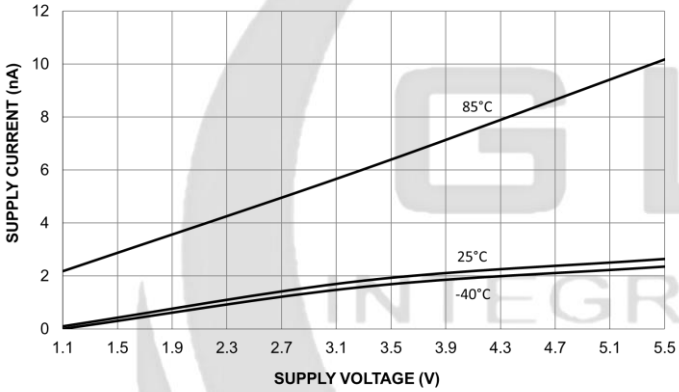


Figure 6. Quiescent Current vs. Supply Voltage

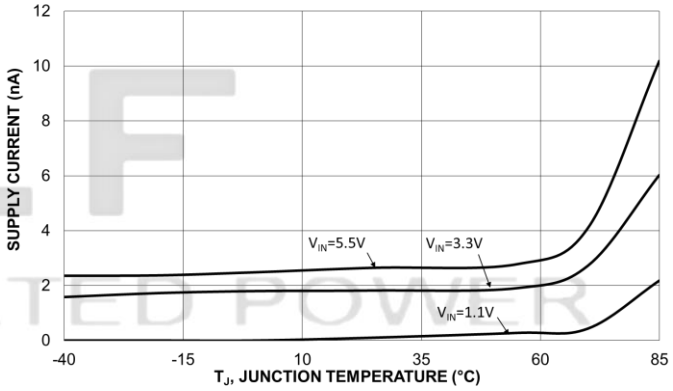


Figure 7. Quiescent Current vs. Temperature

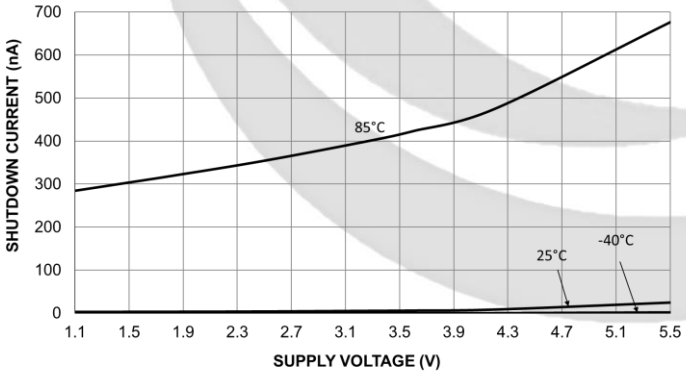


Figure 8. Shutdown Current vs. Input Voltage

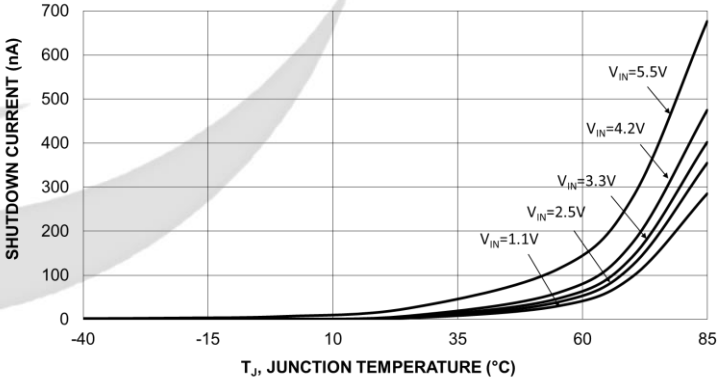


Figure 9. Shutdown Current vs. Temperature

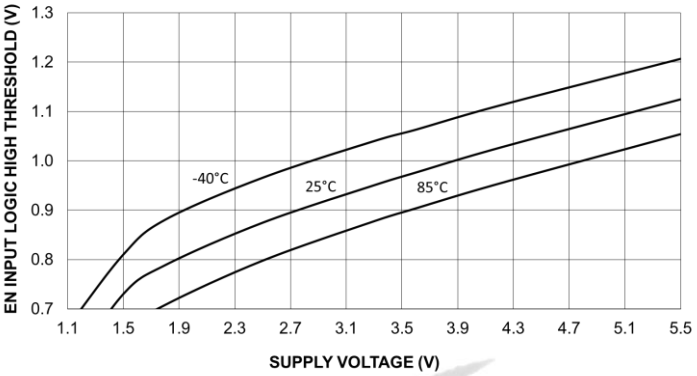


Figure 10. EN Input Logic High Threshold Vs. Temperature

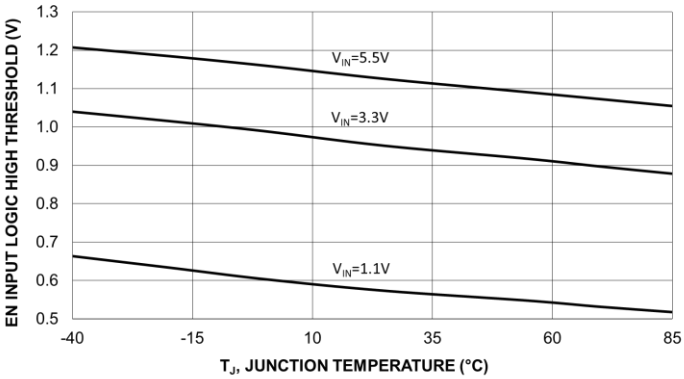


Figure 11. EN Input Logic Low Threshold Vs. Temperature

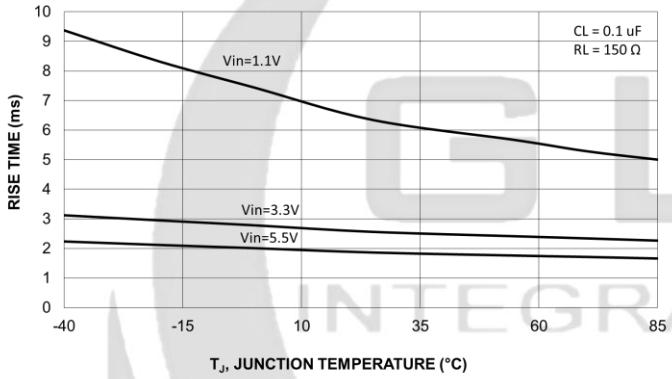


Figure 22. V_{OUT} Rise Time vs. Temperature

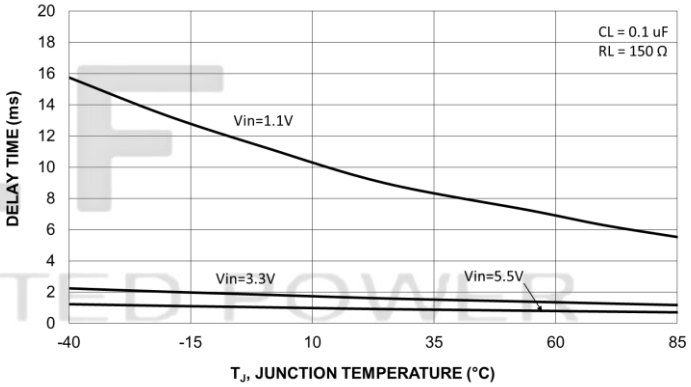


Figure 13. Turn-On Delay Time vs. Temperature

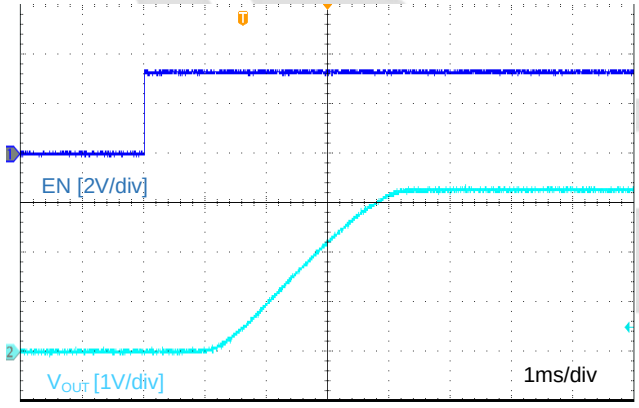


Figure 14. Turn-On Response
V_{IN}=3.3 V, C_{IN}=1.0 uF, C_{OUT}=0.1 uF, R_L=150 Ω

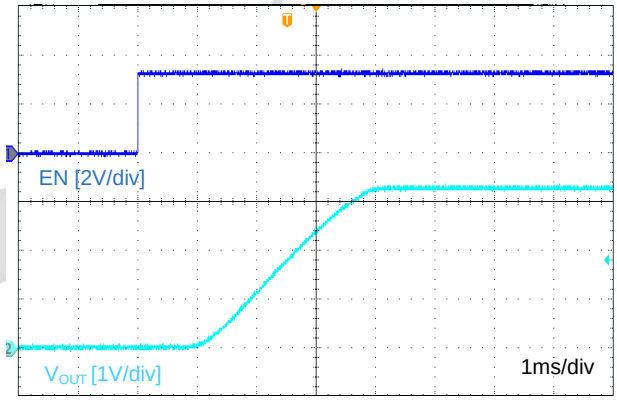


Figure 15. Turn-On Response
V_{IN}=3.3 V, C_{IN}=1.0 uF, C_{OUT}=0.1 uF, R_L=500 Ω

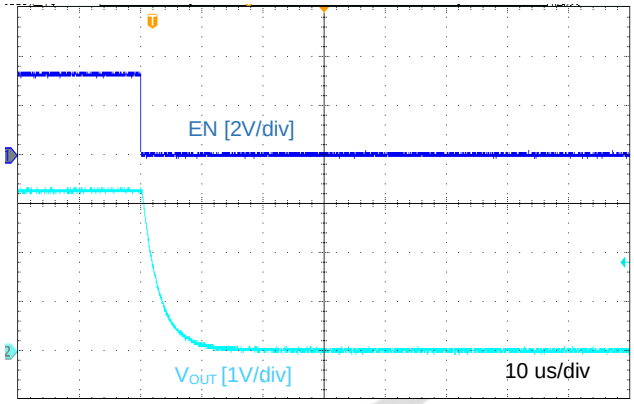


Figure 16. Turn-Off Response, Output Discharge
V_{IN}=3.3 V, C_{IN}=1.0 uF, C_{OUT}=0.1 uF, R_L=150 Ω

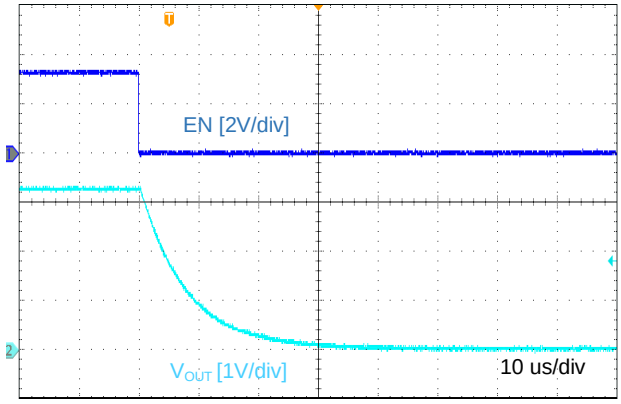


Figure 17. Turn-Off Response, Output Discharge
V_{IN}=3.3 V, C_{IN}=1.0 uF, C_{OUT}=0.1 uF, R_L=500 Ω

APPLICATION INFORMATION

The GLF1100 integrated 2 A, Ultra-Efficient I_QSmart™ Load Switch devices with a fixed slew rate control to limit the inrush current during turn on. Each device is capable of operating over a wide input range from 1.1 V to 5.5 V with very low on-resistance to reduce conduction loss. In the off state, these devices consume very low leakage current to avoid unwanted standby current and save limited input power.

Input Capacitor

The GLF1100 does not require an input capacitor. However, to reduce the voltage drop on the input power rail caused by transient inrush current at start-up, a 0.1 uF capacitor is recommended to be placed close to the V_{IN} pin. A higher input capacitor value can be used to further attenuate the input voltage drop.

Output Capacitor

The GLF1100 does not require an output capacitor. However, use of an output capacitor is recommended to mitigate voltage undershoot on the output pin when the switch is turning off. Undershoot can be caused by parasitic inductance from board traces or intentional load inductances. If load inductances do exist, use of an output capacitor can improve output voltage stability and system reliability. The C_{OUT} capacitor should be spaced close to the VOUT and GND pins.

EN pin

The GLF1100 can be activated by forcing EN pin high level. Note that the EN pin has an internal pull-down resistor to help pull the main switch to a known “off state” when no EN signal is applied from an external controller.

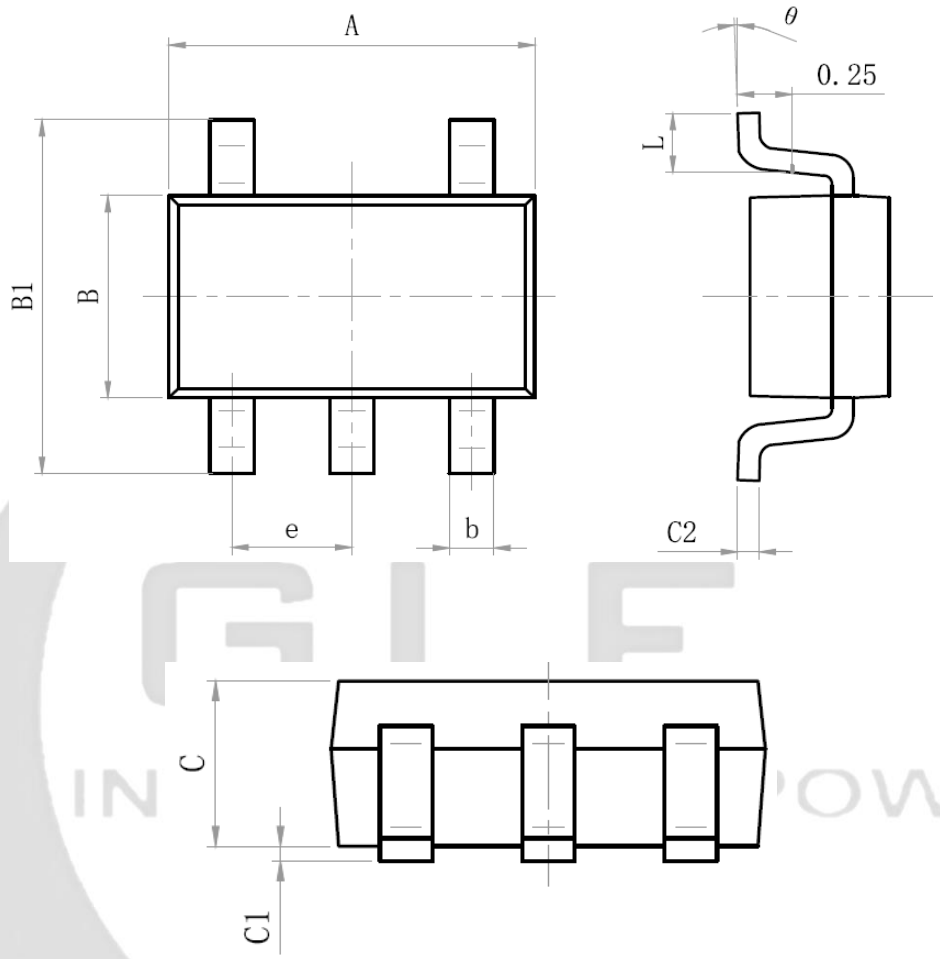
Output Discharge Function

The GLF1100 has an internal discharge N-channel FET switch on the VOUT pin. When EN signal turns the main power FET to an off state, the N-channel switch turns on to discharge an output capacitor quickly.

Board Layout

All traces should be as short as possible to minimize parasitic inductance effects. Wide traces for VIN, VOUT, and GND will help reduce signal degradation and parasitic effects during dynamic operation as well as improve the thermal performance at high load current.

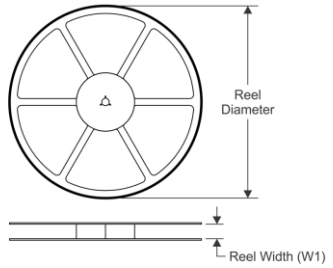
PACKAGE OUTLINE



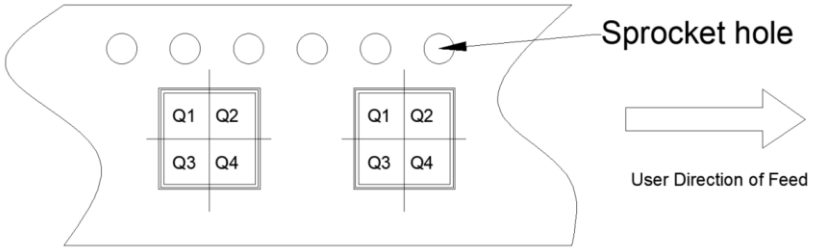
Size / Mark	Min(mm)	Max(mm)	Size / Mark	Min(mm)	Max(mm)
A	2.82	3.02	C	1.05	1.15
e	0.95 (BSC)		C1	0.03	0.15
b	0.28	0.45	C2	0.12	0.23
B	1.50	1.70	L	0.35	0.55
B1	2.60	3.00	θ	0°	8°

TAPE AND REEL INFORMATION

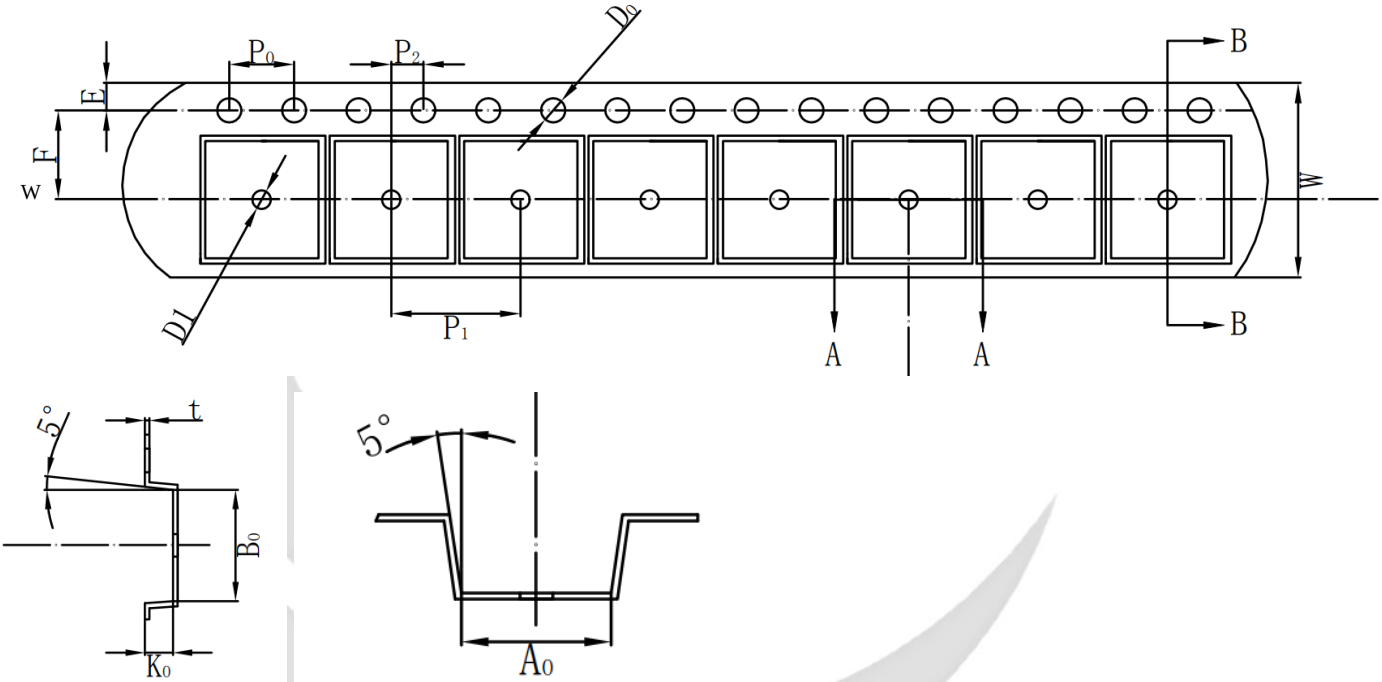
REEL DIMENSIONS



QUADRANT ASSIGNMENTS PIN 1 ORIENTATION TAPE



TAPE DIMENSIONS



Device	Package	Pins	SPQ	Reel Diameter(mm)	Reel Width W1	A0	B0	K0	P1	W	Pin1
GLF1100-T1G7	SOT23-5	5	3000	178	9	3.25	3.30	1.38	4	8	Q3

Remark:

A0: Dimension designed to accommodate the component width

B0: Dimension designed to accommodate the component length

C0: Dimension designed to accommodate the component thickness

W: Overall width of the carrier tape

P1: Pitch between successive cavity centers

SPECIFICATION DEFINITIONS

Document Type	Meaning	Product Status
Target Specification	This is a target specification intended to support exploration and discussion of critical needs for a proposed or target device. Spec limits including typical, minimum, and maximum values are desired, or target, limits. GLF reserves the right to change limits at any time without warning or notification. A target specification in no way guarantees future production of the device in question.	Design / Development
Preliminary Specification	This is a draft version of a product specification. The specification is still under internal review and subject to change. GLF reserves the right to change the specification at any time without warning or notification. A preliminary specification in no way guarantees future production of the device in question.	Qualification
Product Specification	This document represents the anticipated production performance characteristics of the device.	Production

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