GLF1501

3 A Ultra Low Current Consumption N-channel Load Switch with Lower Input Voltage Range and Reverse Current Blocking

Product Specification

DESCRIPTION

The GLF1501 load Switch is a fully integrated 3 A NMOS load switch with I_QSmart™ advanced technology. The device is targeted for the mobile computing and data storage markets as a high performance, low-cost solution for load switch applications.

The GLF1501 has a constant low on-resistance of 52 mΩ at room temperature. The fixed rise time helps prevent undesirable inrush current when turned on and the internal EN pin pulldown resistor ensures the device remains in the shutdown mode when disabled. In shutdown mode the GLF1501 draws only 6 nA typical at 3.6 V input supply voltage.

The GLF1501 features a reverse current blocking protection. When the GLF1501 is disabled, it prevents reverse current flowing from the output to the input source.

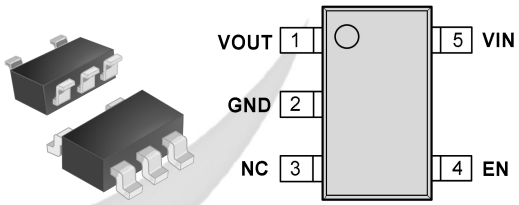
FEATURES

- Supply Voltage Range: 0.85 V to 3.6 V
- Low R_{ON}: 52 mΩ Typ at Supply Voltage Range
- I_{OUT} Max: 3 A
- Ultra-Low I_Q:
  - 50 nA Typ at 0.85 V_{IN}
  - 60 nA Typ at 1.0 V_{IN}
  - 120 nA Typ at 1.5 V_{IN}
- Integrated Slew Rate Control Driver
- Reverse Current Blocking Protection When Disabled
- Internal EN Pull-Down Resistor
- Integrated Output Discharge Switch
- HBM: 4 kV, CDM: 2 kV

APPLICATIONS

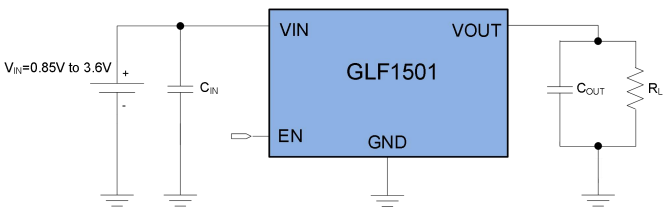
- Low Power Subsystems
- Wearables
- Data Storage

PACKAGE



SOT23-5L

APPLICATION DIAGRAM



ALTERNATE DEVICE OPTIONS

Part Number	Top Mark	R_{ON} (Typ) at Vin Range	Output Discharge	EN Activity
GLF1501-T1G7	FC	52 mΩ	85 Ω	High

FUNCTIONAL BLOCK DIAGRAM

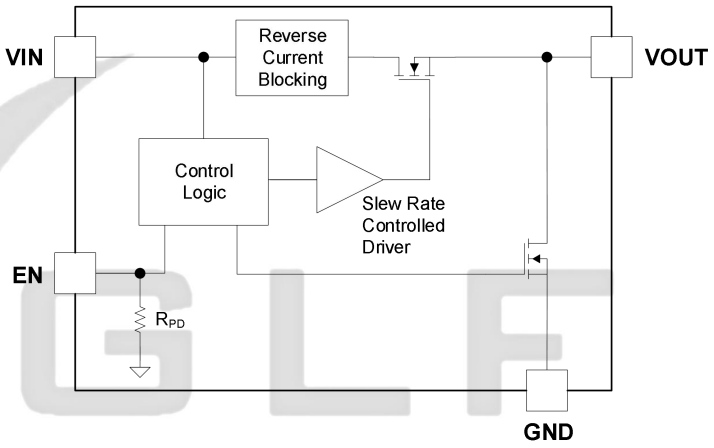


Figure 1. Functional Block Diagram

PIN CONFIGURATION

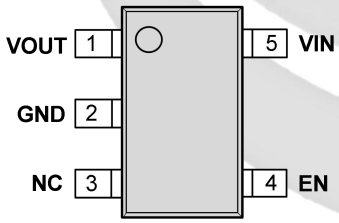


Figure 2. SOT23-5L

PIN DEFINITION

Pin #	Name	Description
1	V_{OUT}	Switch Output
2	GND	Ground
3	NC	No connection
4	EN	Enable to control the switch
5	V_{IN}	Switch Input. Supply Voltage for IC

ABSOLUTE MAXIMUM RATINGS

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
V_{IN}	V_{IN}, V_{OUT}, V_{EN} to GND	-0.3	4	V
I_{OUT}	Maximum Continuous Switch Current		3	A
P_D	Power Dissipation at T_A = 25°C		1	W
T_{STG}	Storage Junction Temperature	-65	150	°C
T_A	Operating Temperature Range	-40	85	°C
θ_{JC}	Thermal Resistance, Junction to Case		90	°C/W
θ_{JA}	Thermal Resistance, Junction to Ambient (Measured using 2S2P JEDEC std. PCB.)		180	°C/W

ESD Ratings

Symbol	Parameter		Value	Unit
HBM	Electrostatic Discharge Capability	Human Body Model, JESD22-A114	4	kV
CDM		Charged Device Model, JESD22-C101	2	

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Max.	Unit
V_{IN}	Supply Voltage	0.85	3.6	V
T_A	Ambient Operating Temperature	-40	+85	°C

ELECTRICAL CHARACTERISTICS

V_{IN} = 0.85 V to 3.6 V and T_A = 25 °C unless otherwise noted.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Units
Basic Operation							
I_Q	Quiescent Current	EN = Enable, I_{OUT} = 0 mA, V_{IN} = 0.85 V			50		nA
		EN = Enable, I_{OUT} = 0 mA, V_{IN} = 1.0 V			60		
		EN = Enable, I_{OUT} = 0 mA, V_{IN} = 1.5 V			120		
		EN = Enable, I_{OUT} = 0 mA, V_{IN} = 2.5 V			7		µA
		EN = Enable, I_{OUT} = 0 mA, V_{IN} = 3.0 V			16		
		EN = Enable, I_{OUT} = 0 mA, V_{IN} = 3.3 V			22		
		EN = Enable, I_{OUT} = 0 mA, V_{IN} = 3.6 V			30		
		EN = Enable, I_{OUT} = 0 mA, V_{IN} = 3.6 V, Ta = 85 °C			46		
I_{SD}	Shutdown Current	EN = Disable, I_{OUT} = 0 mA, V_{IN} = 0.85 V			4		nA
		EN = Disable, I_{OUT} = 0 mA, V_{IN} = 1.0 V			4		
		EN = Disable, I_{OUT} = 0 mA, V_{IN} = 1.2 V			4		
		EN = Disable, I_{OUT} = 0 mA, V_{IN} = 2.5 V			4		
		EN = Disable, I_{OUT} = 0 mA, V_{IN} = 3.0 V			5		
		EN = Disable, I_{OUT} = 0 mA, V_{IN} = 3.3 V			5		
		EN = Disable, I_{OUT} = 0 mA, V_{IN} = 3.6 V			6	10	
		EN = Disable, I_{OUT} = 0 mA, V_{IN} = 3.6 V, Ta = 85 °C			820	950	
R_{ON}	On-Resistance	V_{IN} = 0.85 V to 3.6 V, I_{OUT} = 300 mA	Ta = 25 °C		52	63	mΩ
			Ta = 85 °C		62	71	
V_{IH}	EN Input Logic High Voltage	V_{IN} = 0.85 V to 1.5 V		0.8			V
		V_{IN} = 1.5 V to 3.6 V		1.1			V
V_{IL}	EN Input Logic Low Voltage	V_{IN} = 0.85 V to 1.5 V				0.2	V
		V_{IN} = 1.5 V 3.6 V				0.5	V
R_{EN}	EN pull down resistance	Internal Resistance			10		MΩ
R_{DSC}	Output Discharge Resistance (1)	EN = GND			85		Ω

Notes: 1. Output discharge path is disabled when main switch is off.

ELECTRICAL CHARACTERISTICS

V_{IN} = 0.85 V to 3.6 V and T_A = 25 °C unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Switching Characteristics (2)						
t_{dON}	Turn-On Delay R_{OUT} = 150 Ω, C_{OUT} = 0.1 μF	V_{IN} = 0.85 V		2200		μs
		V_{IN} = 1.2 V		300		
		V_{IN} = 3.3 V		145		
		V_{IN} = 3.6 V		125		
t_R	V_{OUT} Rise Time R_{OUT} = 150 Ω, C_{OUT} = 0.1 μF	V_{IN} = 0.85 V		3250		
		V_{IN} = 1.2 V		500		
		V_{IN} = 3.3 V		400		
		V_{IN} = 3.6 V		390		
t_{dOFF}	Turn-Off Delay R_{OUT} = 150 Ω, C_{OUT} = 0.1 μF	V_{IN} = 0.85 V		50		
		V_{IN} = 1.2 V		5		
		V_{IN} = 3.3 V		1		
		V_{IN} = 3.6 V		0.6		
t_F	V_{OUT} Fall Time R_{OUT} = 150 Ω, C_{OUT} = 0.1 μF	V_{IN} = 0.85 V		25		
		V_{IN} = 1.2 V		17		
		V_{IN} = 3.3 V		12		
		V_{IN} = 3.6 V		11		

Notes: 2. By design; characterized, not production tested. $t_{ON} = t_{dON} + t_R$, $t_{OFF} = t_{dOFF} + t_F$

TIMING DIAGRAM

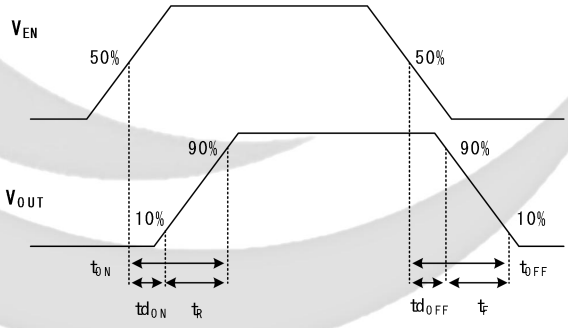


Figure 3. Timing Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

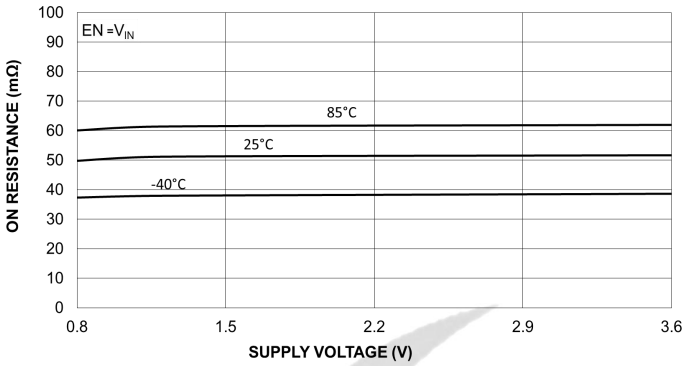


Figure 4. On-Resistance vs. Supply Voltage

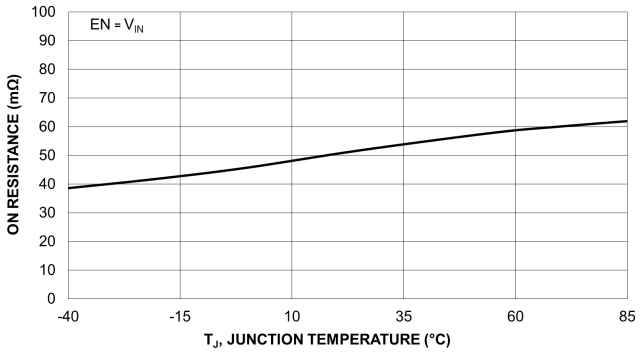


Figure 5. On-Resistance vs. Temperature

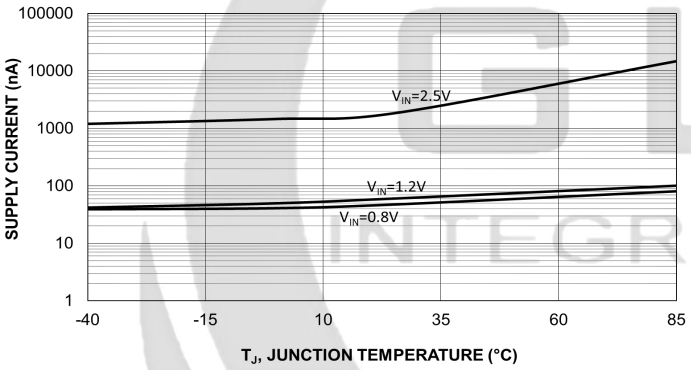


Figure 6. On-Resistance vs. Supply Voltage

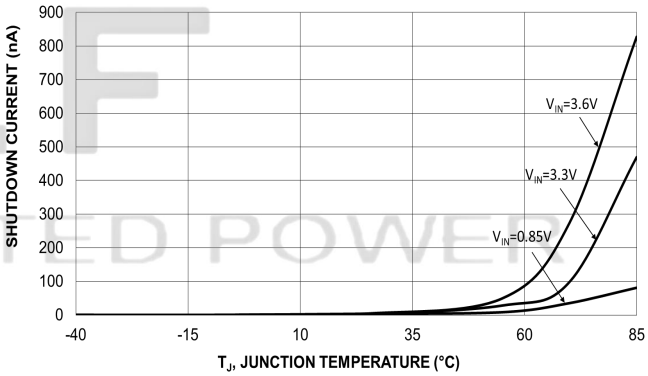


Figure 7. Shutdown Current vs. Supply Voltage

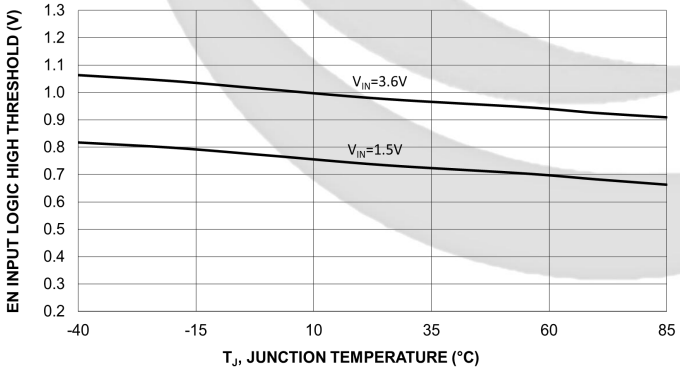


Figure 8. EN Input Logic High Threshold Vs. Temperature

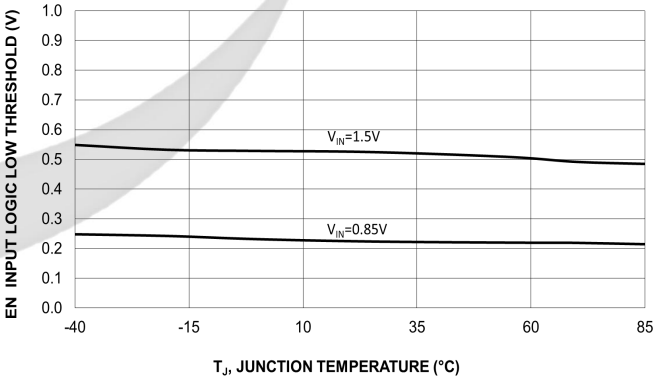


Figure 9. EN Input Logic Low Threshold Vs. Temperature

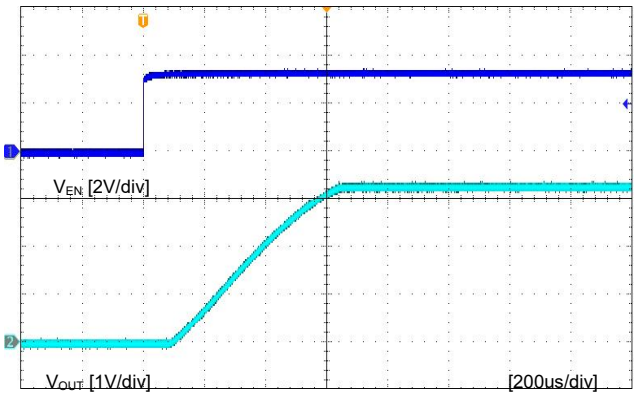


Figure 10. Turn-On Response
V_{IN} = 3.3 V, C_{OUT} = 0.1 uF, R_L = 150 Ω

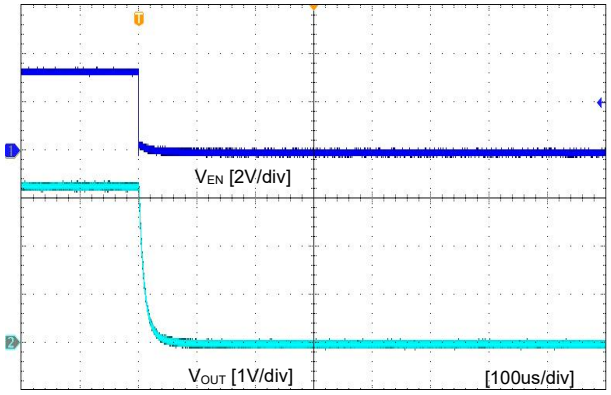


Figure 11. Turn-Off Response, GLF1501
V_{IN} = 3.3 V, C_{OUT} = 0.1 uF, R_L = 150 Ω

APPLICATION INFORMATION

The GLF1501 is a fully integrated 3 A NMOS load switch with fixed slew rate control to limit the inrush current during turn on. Each device is capable of operating over a wide input range from 0.85 V to 3.6 V with very low on-resistance to reduce conduction loss. In the off state, these devices consume very low leakage current, avoiding unwanted standby current from the input power supply.

Input Capacitor

A capacitor is recommended to be placed close to the V_{IN} pin to reduce the voltage drop on the input power rail caused by transient inrush current at start-up. A higher input capacitor value can be used to further attenuate the input voltage drop.

Output Capacitor

An output capacitor is recommended to minimize voltage undershoot on the output pin during the transition when the switch is turned off. Undershoot can be caused by parasitic inductance from board traces or intentional load inductances. If load inductances do exist, use of an output capacitor can improve output voltage stability and system reliability. The C_{OUT} capacitor should be placed close to the VOUT and GND pins.

Reverse Current Blocking

The GLF1501 has a built-in reverse current blocking protection. When the device is disabled, the reverse current blocking protection is activated to prevent the reverse current from the Vout to the Vin source.

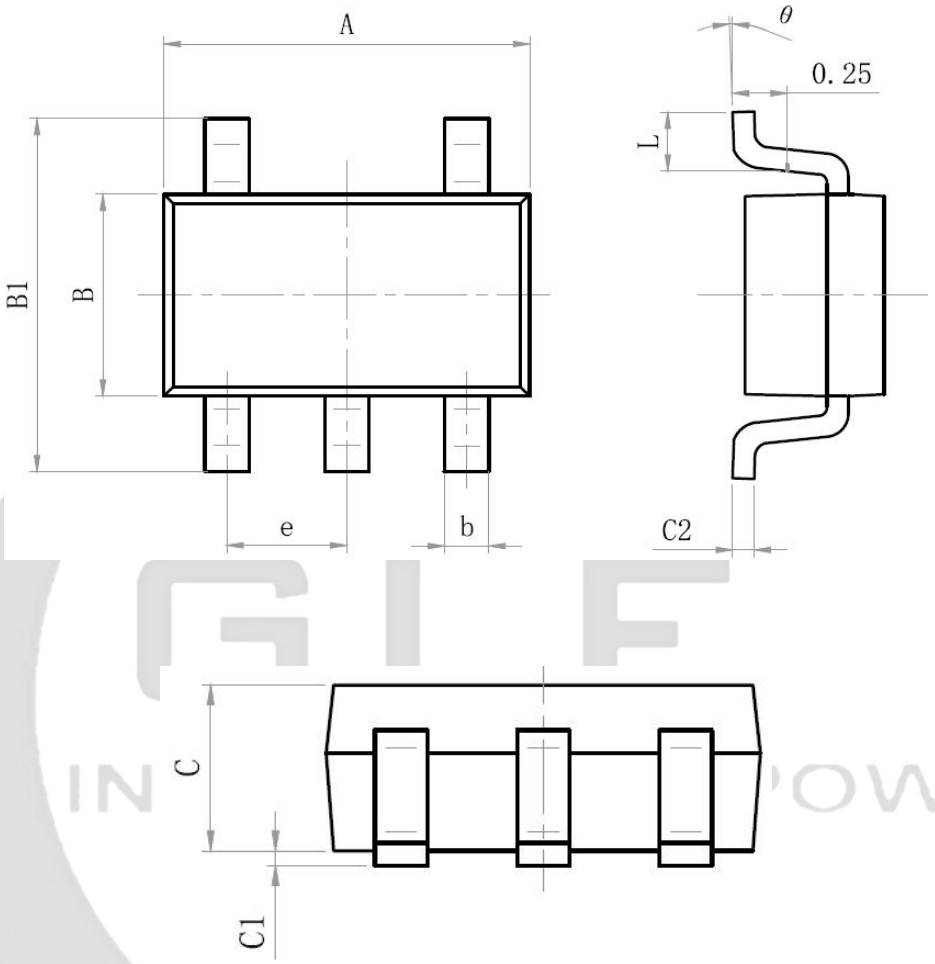
EN pin

The GLF1501 can be activated by EN pin high signal. Note that the EN pin has an internal pull-down resistor to maintain a reliable status without EN signal applied from an external controller.

Board Layout

All traces should be as short as possible to minimize parasitic inductance effect. Wide traces for VIN, VOUT, and GND will help reduce signal degradation and parasitic effects during dynamic operations as well as improve the thermal performance at high load current.

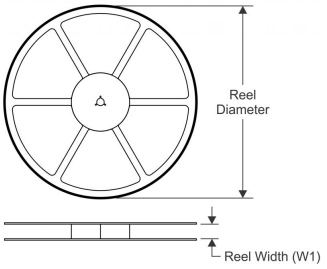
PACKAGE OUTLINE



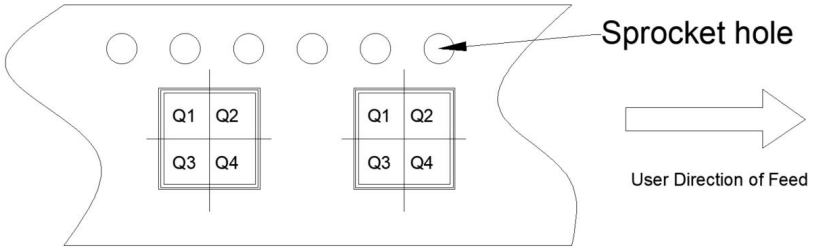
Size / Mark	Min(mm)	Max(mm)	Size / Mark	Min(mm)	Max(mm)
A	2.82	3.02	C	1.05	1.15
e	0.95 (BSC)		C1	0.03	0.15
b	0.28	0.45	C2	0.12	0.23
B	1.50	1.70	L	0.35	0.55
B1	2.60	3.00	θ	0°	8°

TAPE AND REEL INFORMATION

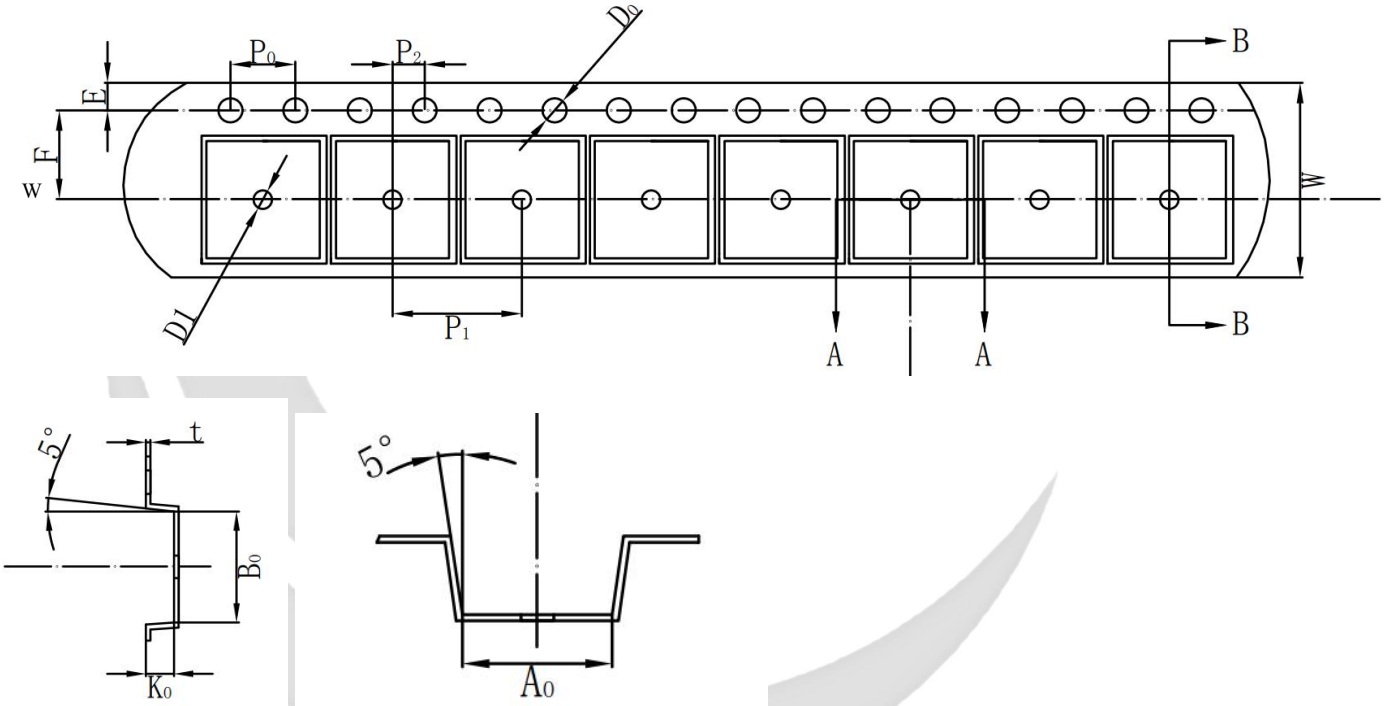
REEL DIMENSIONS



QUADRANT ASSIGNMENTS PIN 1 ORIENTATION TAPE



TAPE DIMENSIONS



Device	Package	Pins	SPQ	Reel Diameter (mm)	Reel Width W1	A0	B0	K0	P1	W	Pin1
GLF1501-T1G7	SOT23-5	5	3000	178	9	3.25	3.30	1.38	4	8	Q3

Remark:

A0: Dimension designed to accommodate the component width

B0: Dimension designed to accommodate the component length

C0: Dimension designed to accommodate the component thickness

W: Overall width of the carrier tape

P1: Pitch between successive cavity centers

SPECIFICATION DEFINITIONS

Document Type	Meaning	Product Status
Target Specification	This is a target specification intended to support exploration and discussion of critical needs for a proposed or target device. Spec limits including typical, minimum, and maximum values are desired, or target, limits. GLF reserves the right to change limits at any time without warning or notification. A target specification in no way guarantees future production of the device in question.	Design / Development
Preliminary Specification	This is a draft version of a product specification. The specification is still under internal review and subject to change. GLF reserves the right to change the specification at any time without warning or notification. A preliminary specification in no way guarantees future production of the device in question.	Qualification
Product Specification	This document represents the anticipated production performance characteristics of the device.	Production

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