GLF1220H, GLF1221H

Nano-Current Consumed, I_QSmart™ Load Switch with Slew Rate Control and True Reverse Current Blocking

Product Specification

DESCRIPTION

The GLF1220H and GLF1221H are an ultra-efficiency, 1 A rated, integrated load switch with the slew rate control as well as a true reverse current blocking function. The best-in-class efficiency makes it an ideal choice for use in IoT, mobile, and wearable electronics.

The GLF1220H and GLF1221H feature an ultra-efficient I_QSmart™ technology that supports the lowest quiescent current (I_Q) and shutdown current (I_{SD}) in the industry. Low I_Q and I_{SD} solutions help designers to reduce parasitic leakage current, improve system efficiency, and increase battery lifetime.

The GLF1220H and GLF1221H offer and industry leading true reverse current blocking (TRCB) function in on and off states. The integrated slew rate control can enhance system reliability by mitigating bus voltage swings during switching events. Where uncontrolled switches can generate high inrush currents that result in voltage droop and/or bus reset events, the GLF1220H and GLF1221H slew rate control specifically limits inrush current during turn-on to minimize voltage droop.

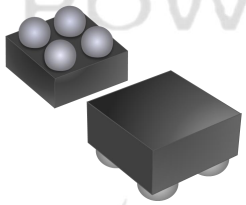
FEATURES

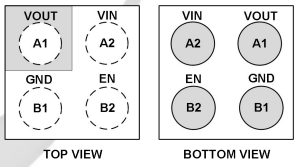
- Wide Input Range, V_{IN} = 1.5 V to 5.5 V
  6 V_{ABS} Max
- I_{OUT} Max = 1 A
- Low R_{ON} = 52 mΩ Typ. at 5.5 V_{IN}
- Ultra-Low I_Q: 500 nA Typ at 5.5 V_{IN}
- Ultra-Low I_{SD}: 10 nA Typ at 5.5 V_{IN}
- True Reverse Current Blocking Protection
- Integrated Output Discharge Switch, GLF1221H
- Internal Pull-Down Resistor on EN Pin

APPLICATIONS

- Wearables
- Mobile Devices
- Low Power Subsystems

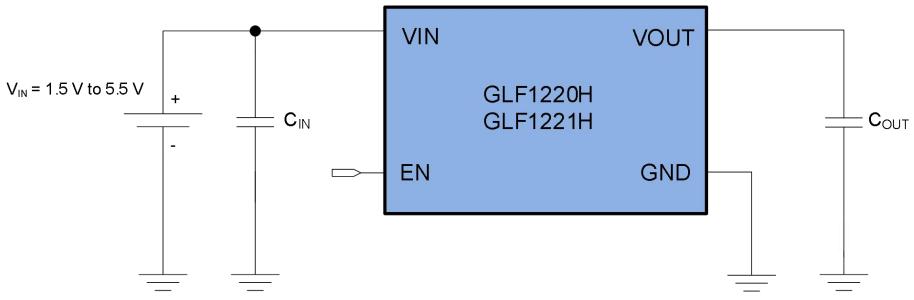
PACKAGE





0.67 mm x 0.67 mm x 0.425 mm
0.35 mm Pitch WLCSP

APPLICATION DIAGRAM



ALTERNATE DEVICE OPTIONS

Part Number	Top Mark	R_{ON} (Typ) at V_{IN} (MAX)	True Reverse Current Blocking	V_{OUT} Rise Time at 3.3 V_{IN}	Output Discharge	EN Activity
GLF1220H	Z	52 mΩ	Yes	390 µs	NA	High
GLF1221H	R				85 Ω	

FUNCTIONAL BLOCK DIAGRAM

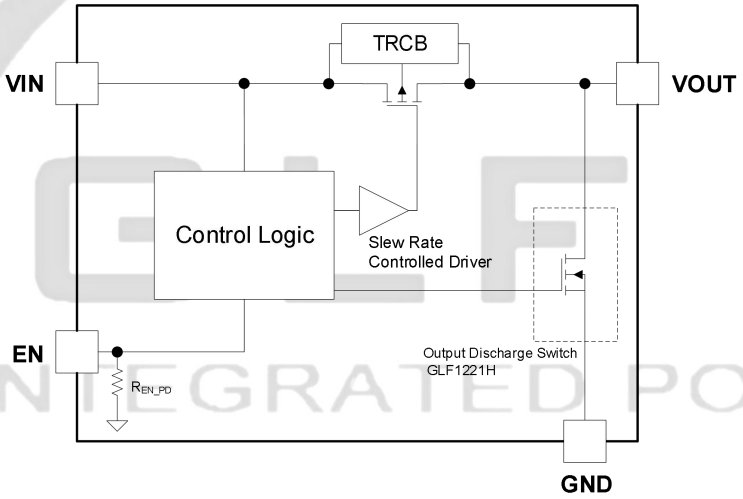


Figure 1. Functional Block Diagram

PIN CONFIGURATION

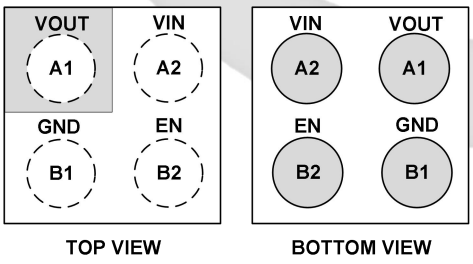


Figure 2. 0.67 mm x 0.67 mm x 0.425 mm WLCSP

PIN DEFINITION

Pin #	Name	Description
A1	V_{OUT}	Switch Output
A2	V_{IN}	Switch Input. Supply Voltage for IC
B1	GND	Ground
B2	EN	Enable to control the switch. The EN pin has an internal pull-down resistor.

ABSOLUTE MAXIMUM RATINGS

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions; extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{IN}, V_{OUT}, V_{EN}	Each Pin Voltage Range to GND		-0.3	6	V
I_{OUT}	Maximum Continuous Switch Current			1	A
	Pulse, 300 us pulse and 2 % duty cycle			2	
P_D	Power Dissipation at T_A = 25 °C			1	W
T_{STG}	Storage Junction Temperature		-65	150	°C
T_A	Operating Temperature Range		-40	85	°C
θ_{JA}	Thermal Resistance, Junction to Ambient (board dependent)			125	°C/W
ESD	Electrostatic Discharge Capability	Human Body Model, JESD22-A114	3		kV
		Charged Device Model, JESD22-C101	2		

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Max.	Unit
V_{IN}	Supply Voltage	1.5	5.5	V
T_A	Ambient Operating Temperature	- 40	+ 85	°C

ELECTRICAL CHARACTERISTICS

Values are at V_{IN} = 3.3 V and T_A = 25 °C unless otherwise noted.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
Basic Operation							
V_{IN}	Supply Voltage			1.5		5.5	V
I_Q (1)	Quiescent Current	V_{IN} =5.5 V, V_{EN} =0 V, I_{OUT}=0 mA			500	680	nA
		V_{IN} =5.5 V, V_{EN} =0 V, I_{OUT}=0 mA, Ta=85 °C (4)			550		
I_{SD}	Shutdown Current	EN = Disable, I_{OUT}=0 mA, V_{IN}=1.5 V			1		
		EN = Disable, I_{OUT}=0 mA, V_{IN}=2.5 V			2		
		EN = Disable, I_{OUT}=0 mA, V_{IN}=3.3 V			3		
		EN = Disable, I_{OUT}=0 mA, V_{IN}=4.5 V			4		
		EN = Disable, I_{OUT}=0 mA, V_{IN}=5.5 V			10	40	
		EN = Disable, I_{OUT}=0 mA, V_{IN}=5.5 V, Ta=55 °C (4)			50		
		EN = Disable, I_{OUT}=0 mA, V_{IN}=5.5 V, Ta=85 °C (4)			275		
R_{ON}	On-Resistance	V_{IN}=5.5 V, I_{OUT}= 500 mA	Ta=25 °C		52	60	mΩ
			Ta=85 °C (4)		60		
		V_{IN}=4.5 V, I_{OUT}= 500 mA	Ta=25 °C		57	65	
			Ta=85 °C (4)		67		
		V_{IN}=3.3 V, I_{OUT}= 500 mA	Ta=25 °C		67	77	
			Ta=85 °C (4)		79		
		V_{IN}=2.5 V, I_{OUT}= 300 mA	Ta=25 °C		82		
		V_{IN}=1.8 V, I_{OUT}= 300 mA	Ta=25 °C		112		
		V_{IN}=1.5 V, I_{OUT}= 100 mA	Ta=25 °C		142		
R_{DSC}	Output Discharge Resistance	V_{EN} = Low , I_{FORCE}= 10 mA, GLF1221H Only			85		Ω
V_{IH}	EN Input Logic High Voltage	V_{IN}=1.5 V to 5.5 V		1.2			V
V_{IL}	EN Input Logic Low Voltage	V_{IN}=1.5 V to 5.5 V				0.3	V
R_{EN}	EN Internal resistance	Internal Pull-down Resistance			10		MΩ
I_{EN}	EN Current (2)	V_{EN} = 5.5 V			0.55	0.8	μA
V_{RCB_TH}	RCB Protection Threshold	V_{OUT} – V_{IN}			40		mV
V_{RCB_RL}	RCB Protection Release	V_{IN} – V_{OUT}			30		
Switching Characteristics (2)							
t_{dON}	Turn-On Delay	R_L=150 Ω, C_{OUT}=0.1 μF			290		μs
t_R	V_{OUT} Rise Time				390		
t_{dOFF}	Turn-Off Delay (3), (4)	R_L=150 Ω, C_{OUT}=0.1 μF GLF1220H			16		
t_F	V_{OUT} Fall Time (3), (4)				30		
t_{dOFF}	Turn-Off Delay (3), (4)	R_L=150 Ω, C_{OUT}=0.1 μF GLF1221H			16		
t_F	V_{OUT} Fall Time (3), (4)				11		

Notes:
1. I_Q does not include the EN pin current through the pull-down resistor R_{EN}.
2. $t_{ON} = t_{dON} + t_R$, $t_{OFF} = t_{dOFF} + t_F$
3. Output discharge path is enabled during off.
4. By design; characterized, not production tested.

TIMING DIAGRAM

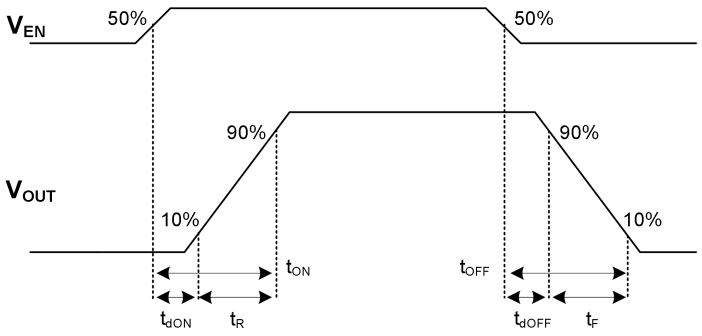


Figure 3. Timing Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

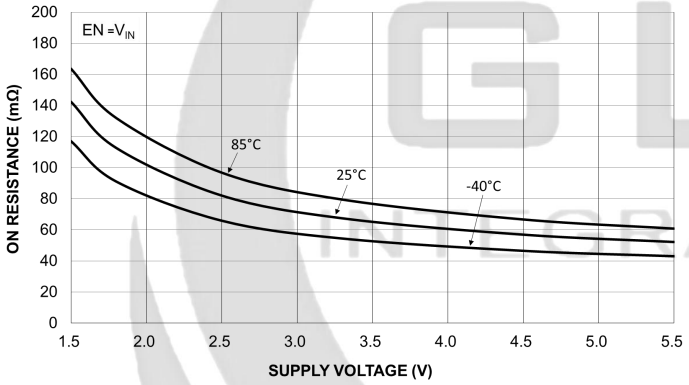


Figure 4. On-Resistance vs. Supply Voltage

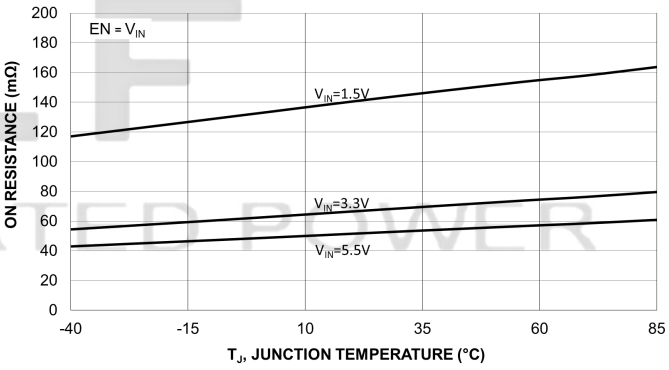


Figure 5. On-Resistance vs. Temperature

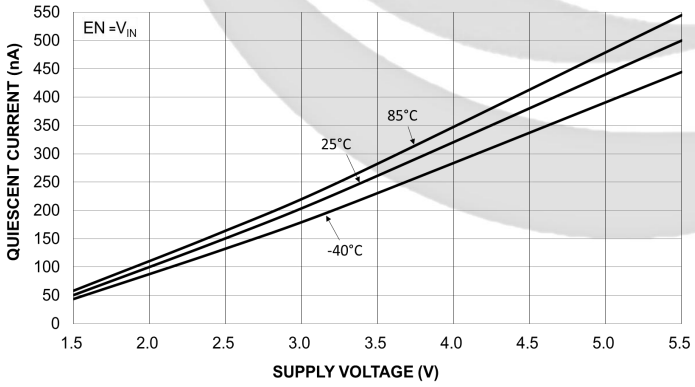


Figure 6. Quiescent Current vs. Supply Voltage

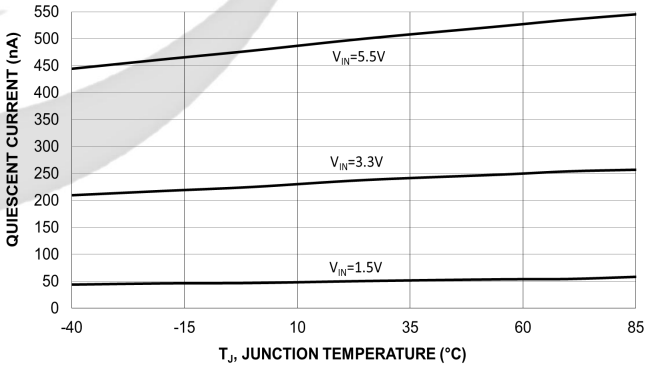


Figure 7. Quiescent Current vs. Temperature

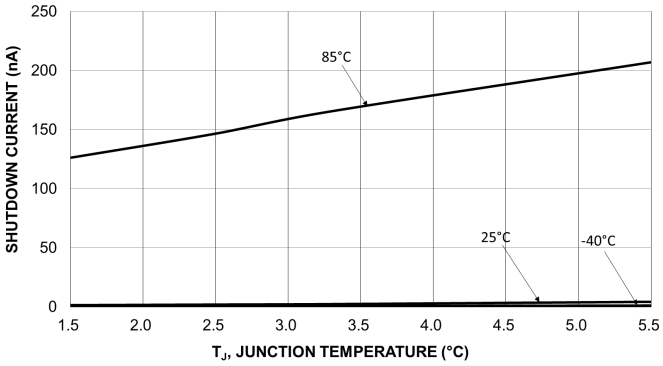


Figure 8. Shutdown Current vs. Supply Voltage

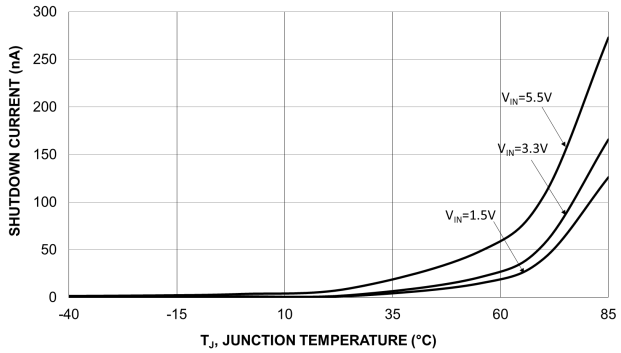


Figure 9. Shutdown Current vs. Temperature

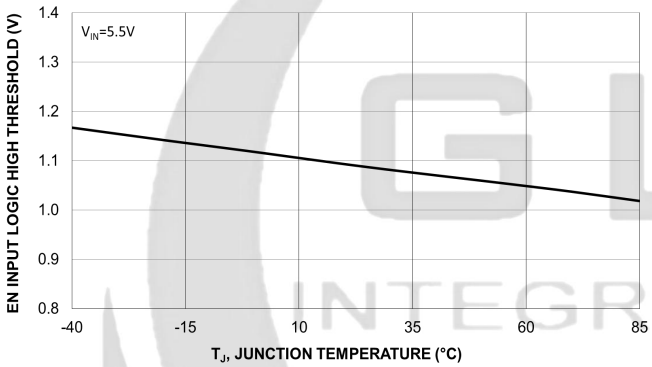


Figure 10. EN Input Logic High Threshold vs. Temperature

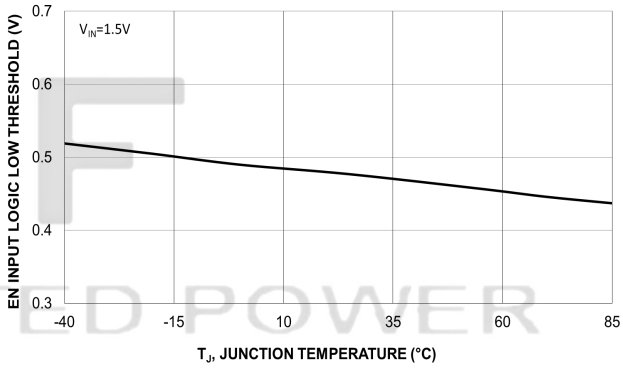


Figure 11. EN Input Logic Low Threshold vs. Temperature

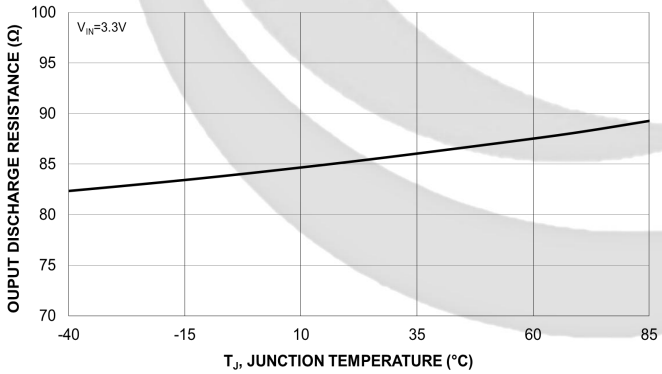


Figure 12. Output Discharge Resistance vs. Temperature GLF1221H

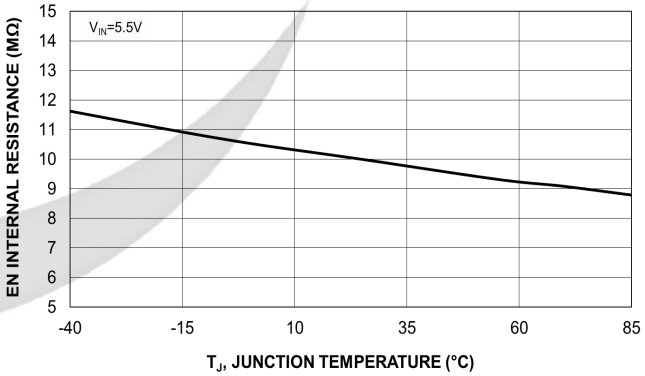


Figure 13. EN Internal Resistance vs. Temperature

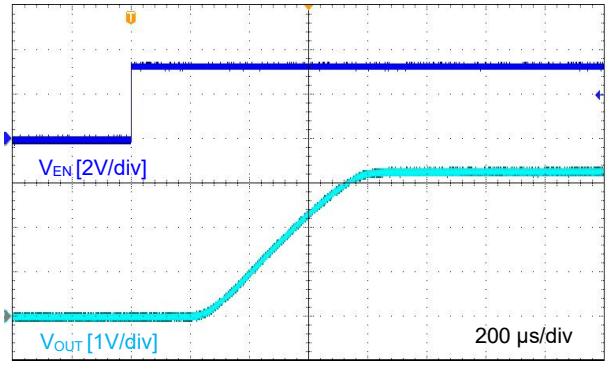


Figure 14. Turn-On Response, GLF1220H
V_{IN}=3.3 V, C_{IN}=1.0 µF, C_{OUT}=0.1 µF, R_L=150 Ω

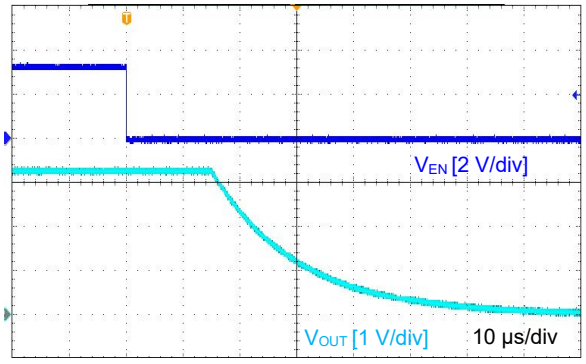


Figure 15. Turn-Off Response, GLF1220H
V_{IN}=3.3 V, C_{IN}=1.0 µF, C_{OUT}=0.1 µF, R_L=150 Ω

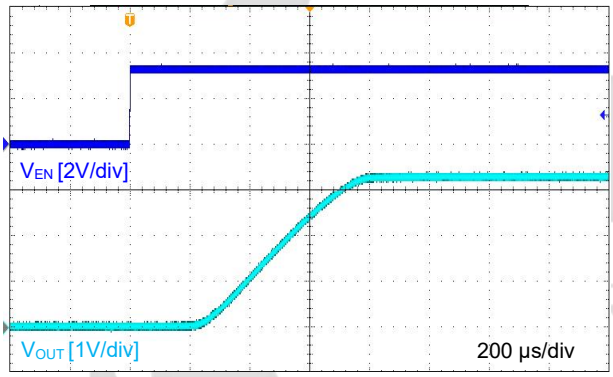


Figure 16. Turn-On Response, GLF1221H
V_{IN}=3.3 V, C_{IN}=1.0 µF, C_{OUT}=0.1 µF, R_L=150 Ω

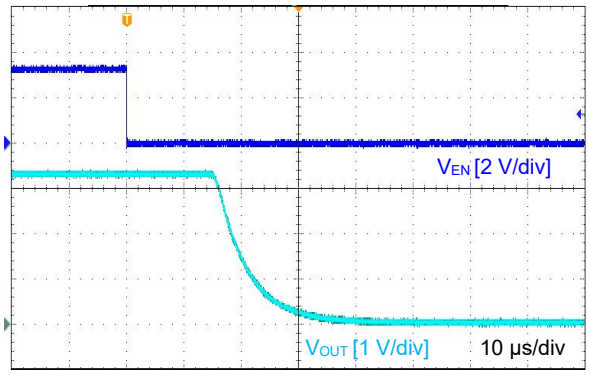


Figure 17. Turn-Off Response, GLF1221H
V_{IN}=3.3 V, C_{IN}=1.0 µF, C_{OUT}=0.1 µF, R_L=150 Ω

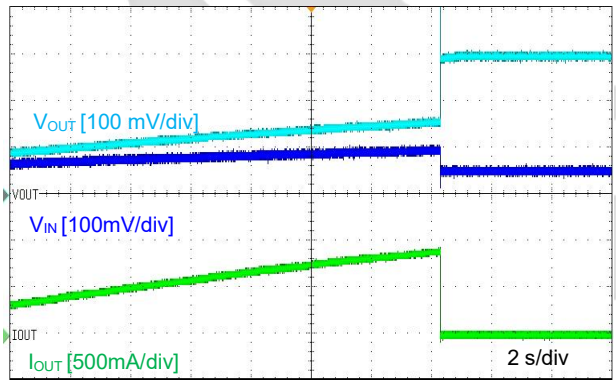


Figure 18. Reverse Current Blocking Threshold
V_{IN}= 3.3 V, V_{OUT} = Up to 3.4 V, C_{IN}= 0.1 µF, C_{OUT}=0.1 µF

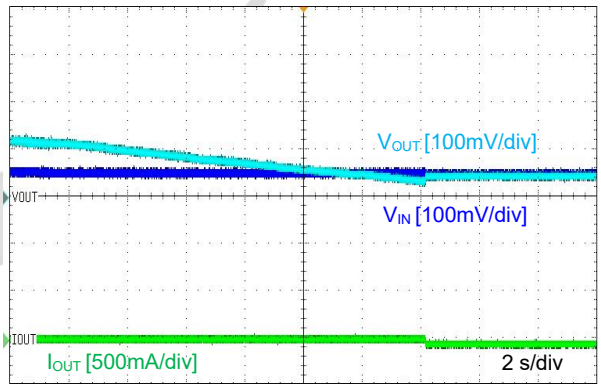


Figure 19. Reverse Current Blocking Release
V_{IN}= 3.3 V, V_{OUT} = Down to 3.2 V, C_{IN}= 0.1 µF, C_{OUT}=0.1 µF

APPLICATION INFORMATION

The GLF1220H and GLF1221H are an integrated 1 A, ultra-efficient I_QSmart™ load switch devices with a fixed slew rate control to limit the inrush current during turn on. Each device is capable of operating over a wide input range from 1.5 V to 5.5 V with very low on-resistance to reduce conduction loss. In the off state, these devices consume very low leakage current to avoid unwanted standby current and save limited input power. The package is a 0.67 mm x 0.67 mm x 0.425 mm wafer level chip scale package, saving space in compact applications. It is constructed using 4 bumps, with a 0.35 mm pitch for manufacturability.

Input Capacitor

The GLF1220H and GLF1221H do not require an input capacitor. However, to reduce the voltage drop on the input power rail caused by transient inrush current at start-up, a 0.1 µF capacitor is recommended to be placed close to the VIN pin. A higher input capacitor value can be used to further attenuate the input voltage drop.

Output Capacitor

The GLF1220H and GLF1221H do not require an output capacitor. However, use of an output capacitor is recommended to mitigate voltage undershoot on the output pin when the switch is turning off. Undershoot can be caused by parasitic inductance from board traces or intentional load inductances. If load inductances do exist, use of an output capacitor can improve output voltage stability and system reliability. The C_{OUT} capacitor should be spaced close to the VOUT and GND pins.

EN pin

The GLF1220H and GLF1221H can be activated by forcing EN pin high level. Note that the EN pin has an internal pull-down resistor to help pull the main switch to a known “off state” when no EN signal is applied from an external controller.

True Reverse Current Blocking

The GLF1220H and GLF1221H have a built-in reverse current blocking protection which always monitors the output voltage level regardless of the status of EN pin to check if it is greater than the input voltage. When the output voltage goes beyond the RCB protection threshold (V_{RCB_TH}), the reverse current blocking function block turns off the switch. Note that some reverse current can occur until the V_{RCB} is triggered. The main switch will resume normal operation when the output voltage drops below the input source by the RCB protection release voltage (V_{RCB_RL}).

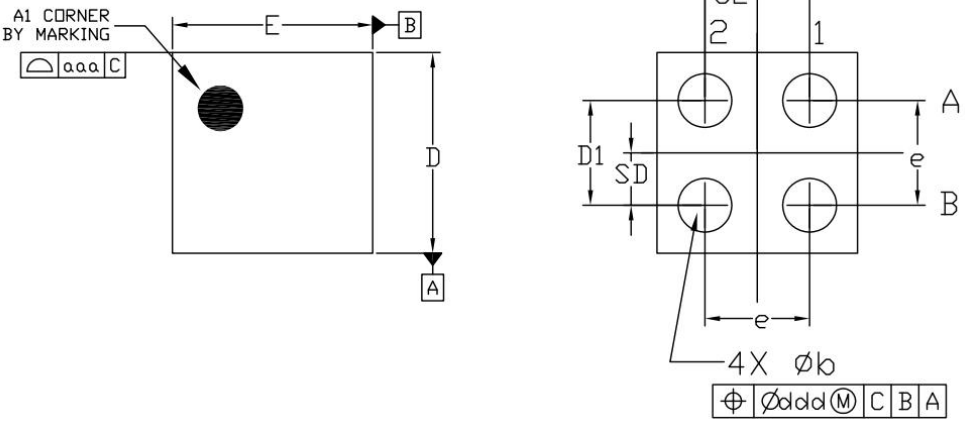
Output Discharge Function

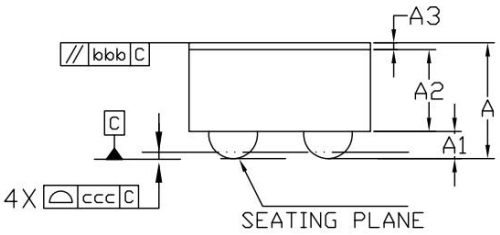
The GLF1221H has an internal discharge N-channel FET switch on the VOUT pin. When EN signal turns the main power FET to an off state, the N-channel switch turns on to discharge an output capacitor quickly.

Board Layout

All traces should be as short as possible to minimize parasitic inductance effects. Wide traces for VIN, VOUT, and GND will help reduce signal degradation and parasitic effects during dynamic operation as well as improve the thermal performance at high load current.

PACKAGE OUTLINE





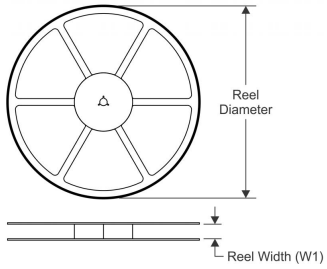
Dimensional Ref.			
REF.	Min.	Nom.	Max.
A	0.380	0.425	0.470
A1	0.085	0.100	0.115
A2	0.275	0.300	0.325
A3	0.020	0.025	0.030
D	0.655	0.670	0.685
E	0.655	0.670	0.685
D1	0.300	0.350	0.400
E1	0.300	0.350	0.400
b	0.145	0.180	0.215
e	0.350 BSC		
SD	0.175 BSC		
SE	0.175 BSC		
Tol. of Form&Position			
aaa	0.10		
bbb	0.10		
ccc	0.05		
ddd	0.05		

Notes

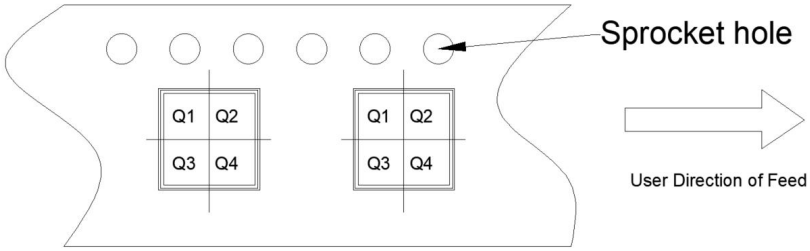
1. ALL DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGRESS)
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.
3. A3: BACKSIDE LAMINATION

TAPE AND REEL INFORMATION

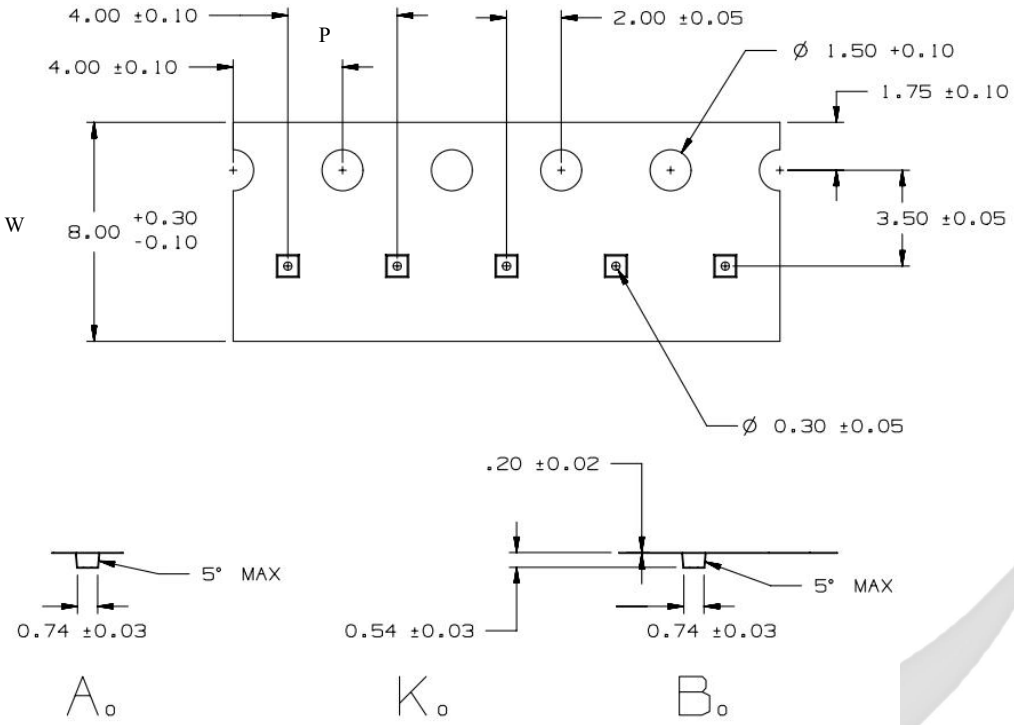
REEL DIMENSIONS



QUADRANT ASSIGNMENTS PIN 1 ORIENTATION TAPE



TAPE DIMENSIONS



Device	Package	Pins	SPQ	Reel Diameter (mm)	Reel Width W1	A0	B0	K0	P	W	Pin1
GLF1220H	WLCSP	4	4000	180	9	0.74	0.74	0.54	4	8	Q1
GLF1221H	WLCSP	4	4000	180	9	0.74	0.74	0.54	4	8	Q1

Remark:

A0: Dimension designed to accommodate the component width

B0: Dimension designed to accommodate the component length

C0: Dimension designed to accommodate the component thickness

W: Overall width of the carrier tape

P: Pitch between successive cavity centers

SPECIFICATION DEFINITIONS

Document Type	Meaning	Product Status
Target Specification	This is a target specification intended to support exploration and discussion of critical needs for a proposed or target device. Spec limits including typical, minimum, and maximum values are desired, or target, limits. GLF reserves the right to change limits at any time without warning or notification. A target specification in no way guarantees future production of the device in question.	Design / Development
Preliminary Specification	This is a draft version of a product specification. The specification is still under internal review and subject to change. GLF reserves the right to change the specification at any time without warning or notification. A preliminary specification in no way guarantees future production of the device in question.	Qualification
Product Specification	This document represents the anticipated production performance characteristics of the device.	Production

DISCLAIMERS

Information in this document is believed to be accurate and reliable, however GLF assumes no liability for errors or omissions. Device performance may be impacted by testing methods and application use cases. Users are responsible to independently evaluate the applicability, usability, and suitability of GLF devices in their application. In no case will GLF be liable for incidental, indirect, or consequential damages associated with the use, misuse, or sale of its product. Customers are wholly responsible to assure GLF devices meet their system level and end product requirements. GLF retains the right to change the information provided in this data sheet without notice.