GLF74520

Ultra-Low Current Consumption Power Multiplexer Switch with Auto & Manual Input Selection

Product Specification

DESCRIPTION

The GLF74520 is an integrated power multiplexer switch with dual independent power switches connected to a single output pin to enable seamless transition between two input sources.

The GLF74520 provides an automatic selection mode as well as a manual selection mode by the combination of the logic input pins of EN and SEL. The EN input pin is used along with the select (SEL) input pin to select the automatic switching function, select VIN1 only, select VIN2 only, or turn both switches off. In the automatic selection mode, the GLF74520 automatically selects the higher input voltage source out of two input DC power supplies.

The GLF74520 features an ultra-efficient I_QSmart™ technology that supports the lowest R_{ON}, quiescent current (I_Q) and shutdown current (I_{SD}) in the industry. Low R_{ON} reduces conduction losses, while low I_Q and I_{SD} solutions help designers to reduce parasitic leakage current, improve system efficiency, and increase battery lifetime.

The GLF74520 blocks any cross conduction current between two input sources. When the switch is disabled, the GLF74520 prevents the reverse current to the input source from the output at any higher Vout than Vin condition.

The GLF74520 utilizes chip scale package technology with 6 bumps in a 0.97 mm x 1.47 mm x 0.55 mm package size with a 0.5 mm bump pitch.

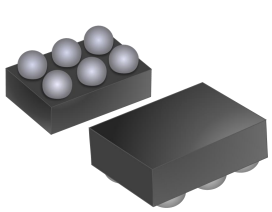
FEATURES

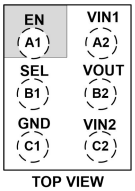
- Two-Input and Single-Output Power Multiplexer Switch
- Automatic and Manual Input Selection Mode
- Supply Voltage Range: 1.5 V to 5.5 V
  6 V_{abs} Max
- R_{ON}: 35 mΩ Typ. at 5.5 V_{IN1} or V_{IN2}
  43 mΩ Typ. at 3.3 V_{IN1} or V_{IN2}
- 2.5 A Continuous Output Current Capability Per Channel
- Ultra-Low Supply Current at Operation
  I_Q: 4 µA Typ at 5.5 V_{IN}
- Ultra-Low Stand-by Current
  I_{SD}: 20 nA Typ at 5.5 V_{IN}
- Smart Control Pins
  I_{EN} and I_{SEL}: 3 nA Typ at V_{EN} or V_{SEL} > V_{IH}
  R_{EN} and R_{SEL}: 500 kΩ Typ
- No Cross Conduction Between Two Inputs
- Reverse Current Blocking when Disabled
- Operating Temperature Range: -40 to 85 °C
- HBM: 6 kV, CDM: 2 kV

APPLICATIONS

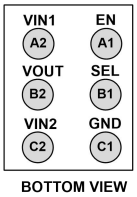
- Wearables / Hearables
- Smart IoT Devices
- Portable Devices

PACKAGE





TOP VIEW



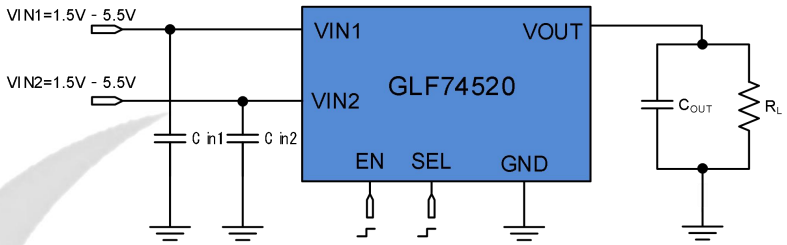
BOTTOM VIEW

0.97mm x 1.47mm x 0.55mm, 0.5mm pitch

DEVICE ORDERING INFORMATION

Part Number	Top Mark	R_{ON} at 5.5 V_{IN}	Output Current, I_{OUT}	Ultra-low I_Q at 5.5 V_{IN}
GLF74520	AR	35 mΩ	2.5 A	4 µA

APPLICATION DIAGRAM



FUNCTIONAL BLOCK DIAGRAM

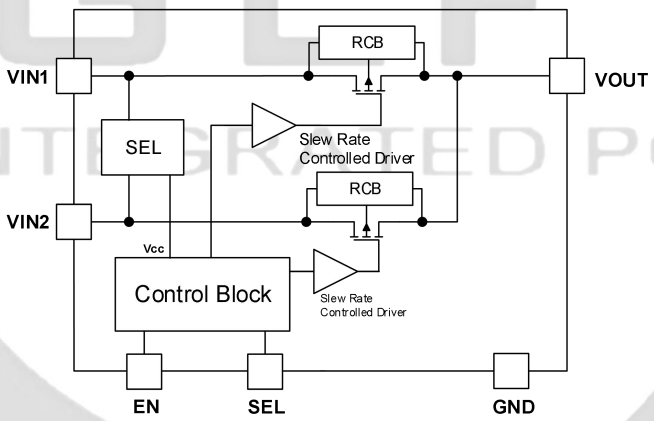


Figure 1. Functional Block Diagram

PIN CONFIGURATION

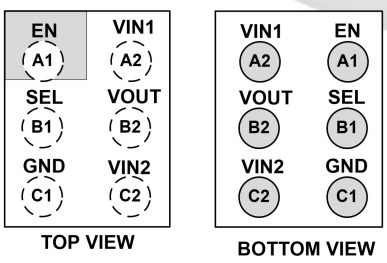


Figure 2. 0.97mm x 1.47mm x 0.55mm WLCSP

PIN DEFINITION

Pin #	Name	Description
A1	EN	Enable to control the switch. Do not leave the EN pin floating.
A2	VIN1	Switch Input 1
B1	SEL	Input Source Selection. Do not leave the SEL pin floating.
B2	VOUT	Switch Output
C1	GND	Ground
C2	VIN2	Switch Input 2

ABSOLUTE MAXIMUM RATINGS

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions; extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{IN1}, V_{IN2} V_{OUT}, EN	Each Pin Voltage Range to GND		-0.3	6	V
I_{OUT}	Maximum Continuous Switch Current			2.5	A
	Pulse, 100 us pulse and 2 % duty cycle			4.5	
P_D	Power Dissipation at T_A = 25°C			1.2	W
T_{STG}	Storage Junction Temperature		-65	150	°C
T_A	Operating Temperature Range		-40	85	°C
θ_{JA}	Thermal Resistance, Junction to Ambient (1)			85	°C/W
ESD	Electrostatic Discharge Capability	Human Body Model, JESD22-A114	6		kV
		Charged Device Model, JESD22-C101	2		

Notes: 1. The thermal resistance depends on the PCB layout and heat dissipation.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Max.	Unit
V_{IN1}, V_{IN2}	Supply Voltage	1.5	5.5	V
T_A	Ambient Operating Temperature	-40	+85	°C

ELECTRICAL CHARACTERISTICS

V_{IN1} = V_{IN2} = 1.5V to 5.5V and T_A = 25°C. Unless otherwise noted

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Units
Basic Operation							
I_{Q1}, I_{Q2}	Quiescent Current	V_{IN1} = 5.5 V, V_{IN2} < V_{in1}, I_{OUT} = 0 mA, EN = 0 V, SEL = V_{IN1}, V_{OUT} = V_{IN1} or V_{IN2} = 5.5 V, V_{IN1} < V_{IN2}, I_{OUT} = 0 mA, EN = SEL = V_{IN2}, V_{OUT} = V_{IN2}			4	5.0	µA
		As above, Ta = 85°C (1)			4.7		
I_{SD1}, I_{SD2}	Shutdown Current	$V_{IN1,2}$ = 5.5 V, V_{OUT} = GND, EN = SEL = 0 V			20	50	nA
		$V_{IN1,2}$ = 5.5 V, V_{OUT} = GND, EN = SEL = 0 V, Ta=85 °C (1)			500		
R_{ON}	On-Resistance	V_{IN1} or V_{IN2} = 5.5 V I_{OUT}= 500 mA	Ta = 25 °C		35	40	mΩ
			Ta = 85 °C (1)		40		
		V_{IN1} or V_{IN2} = 4.5 V, I_{OUT}= 500 mA	Ta = 25 °C		37	42	
			Ta = 85 °C (1)		42		
		V_{IN1} or V_{IN2} = 3.3 V, I_{OUT}= 500 mA	Ta = 25 °C		43	49	
			Ta = 85 °C (1)		50		
		V_{IN1} or V_{IN2} = 2.5 V, I_{OUT}= 300 mA	Ta = 25 °C		51	57	
		V_{IN1} or V_{IN2} = 1.5 V, I_{OUT}= 100 mA	Ta = 25 °C		82		
V_{IH}	EN, SEL Input Logic High Voltage			1.3			V
V_{IL}	EN, SEL Input Logic Low Voltage					0.4	V
I_{EN}, I_{SEL}	EN, SEL Current	V_{EN} or V_{SEL} > V_{IH}, Enabled			3	20	nA
R_{EN}, R_{SEL}	EN, SEL Pulldown Resistance	V_{EN} or V_{SEL} < V_{IL}, Disabled			500		kΩ
I_{RVS}	Reverse Current (1)	V_{IN1} = V_{IN2} =0 V, V_{OUT}=5.5 V, EN=SEL=0 V			2.6		µA
Switching Characteristics (2)							
t_{dON}	Turn-On Delay	V_{IN1} = 5.0 V, V_{IN2} = 3.3V, R_L=150Ω, C_{OUT}=1.0 µF			210		µs
t_R	VOUT Rise Time				350		µs
T_{dHL}	High-low Delay (1)				3		µs
T_{fHL}	High-low Fall Time (1)				6		µs
V_{droop}	Voltage Droop (1)				160		mV
T_{dLH}	Low-high Delay (1)				7		µs
T_{rLH}	Low-high Rise Time (1)				4		µs
t_{dOFF}	Turn-Off Delay (1)				18		µs
t_F	VOUT Fall Time (1)				350		µs

Notes:
1. By design; characterized, not production tested.
2. t_{ON} = t_{dON} + t_R, t_{OFF} = t_{dOFF} + t_F

TIMING DIAGRAM and TRUTH TABLE

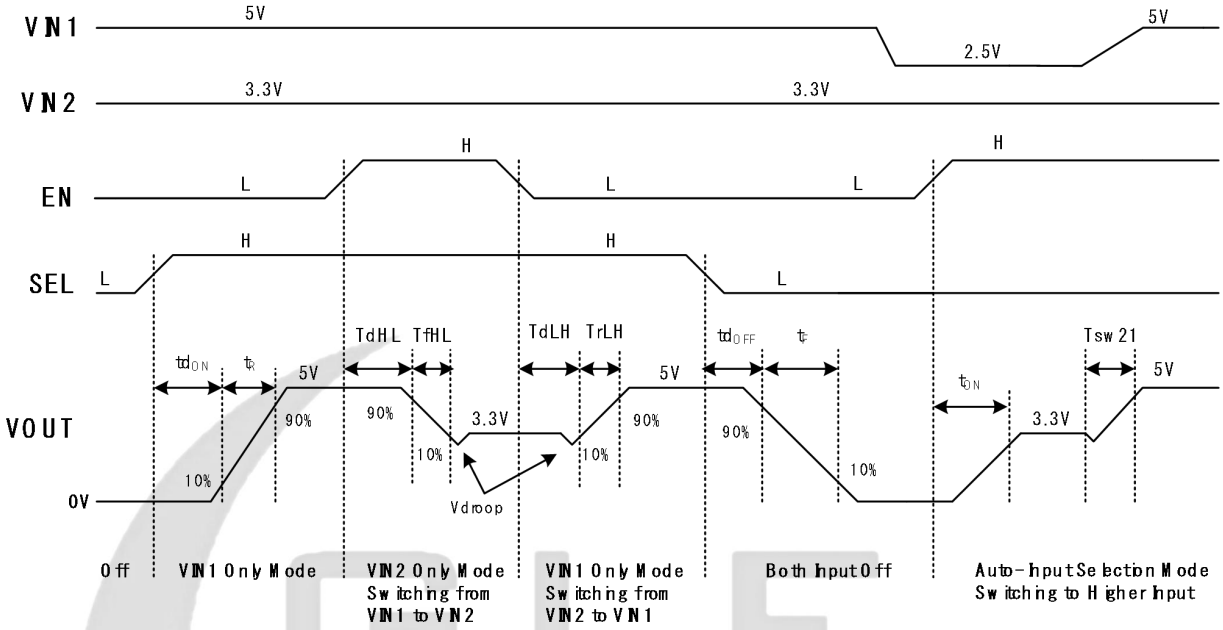


Figure 3. Timing Diagram

SEL	EN	Function	VOUT
0	0	Both switches are off	High-Z
0	1	Auto-Input selection. Vout is connected to a higher input source automatically	Higher Input between V_{IN1} and V_{IN2}
1	0	Only V_{IN1} is selected	V_{IN1}
1	1	Only V_{IN2} is selected	V_{IN2}

Table 1. Truth Table of Input Source Selection

TYPICAL PERFORMANCE CHARACTERISTICS

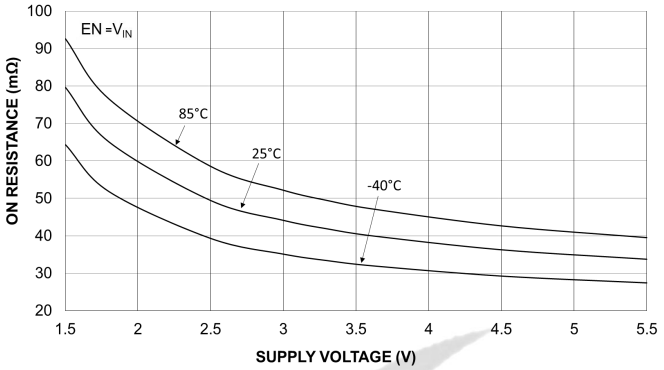


Figure 4. On-Resistance vs. Supply Voltage

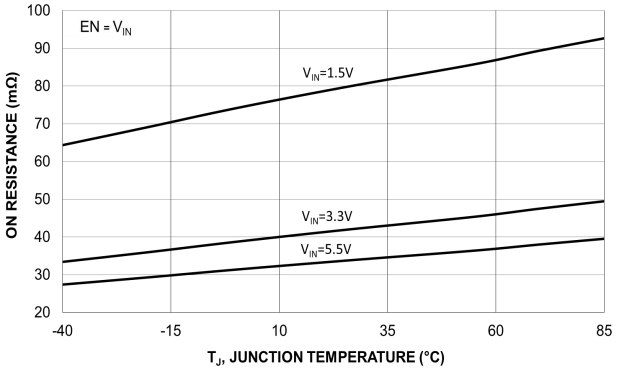


Figure 5. On-Resistance vs. Temperature

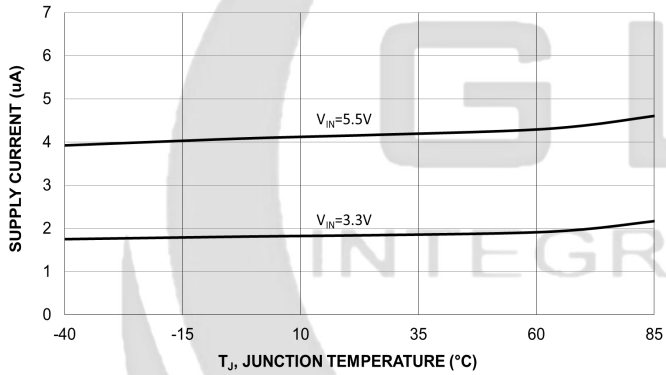


Figure 6. Quiescent Current vs. Temperature

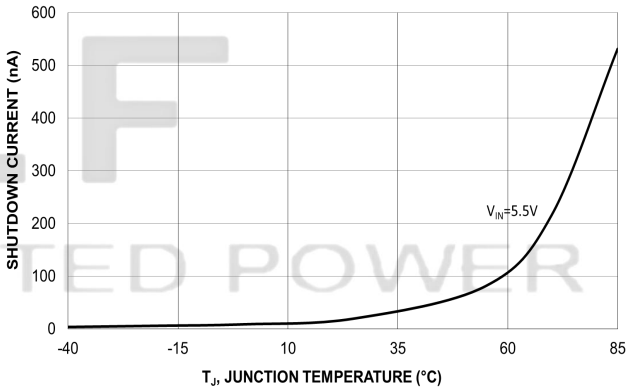


Figure 7. Shutdown Current vs. Temperature

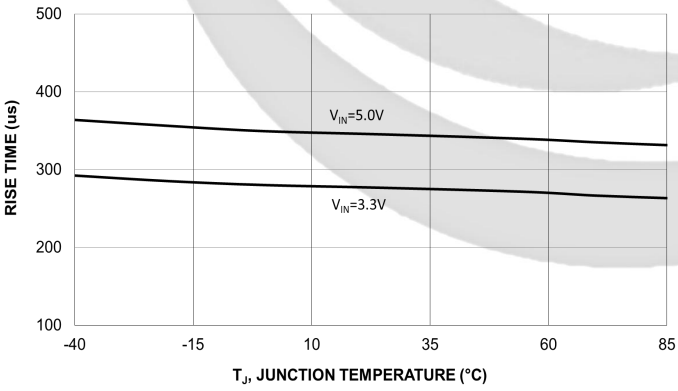


Figure 8. V_{OUT} Rise Time vs. Temperature

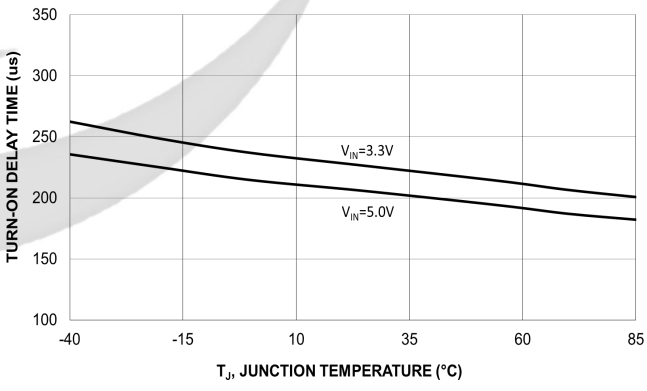


Figure 9. Turn-On Delay Time vs. Temperature

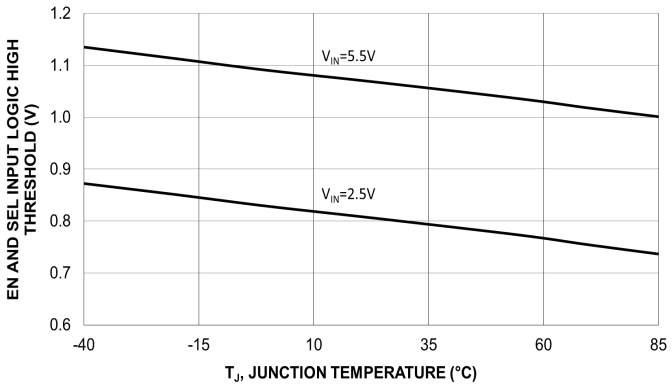


Figure 10. EN and SEL Input Logic High Threshold Vs. Temperature

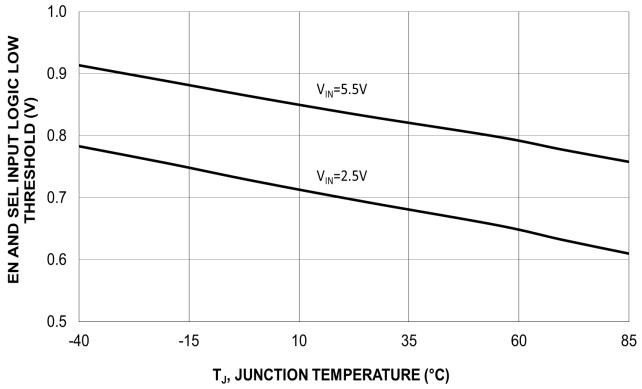


Figure 11. EN and SEL Input Logic Low Threshold Vs. Temperature

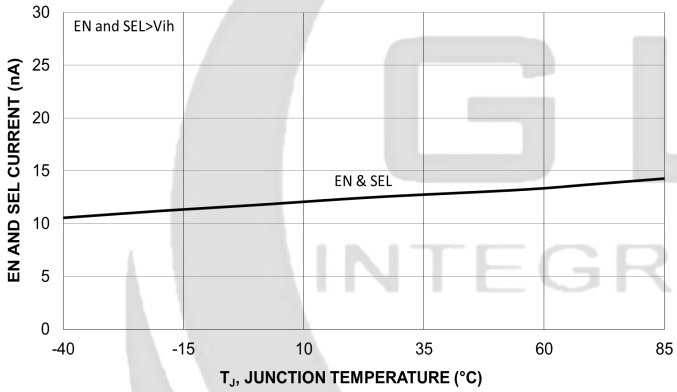


Figure 12. EN and SEL Current vs. Temperature

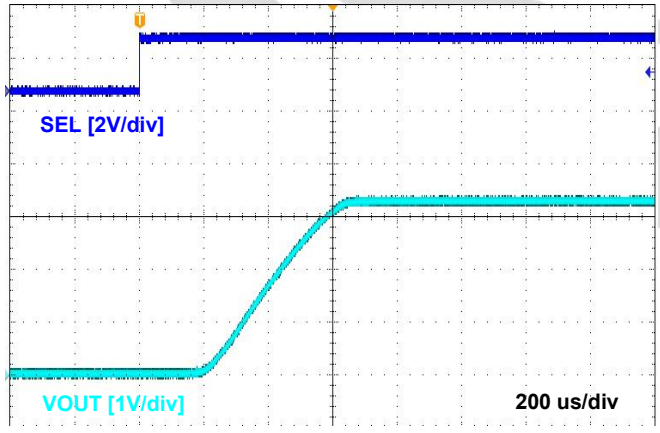


Fig Figure 13. Turn-On Response
V_{IN1}=3.3 V, C_{IN}=0.1 µF, C_{OUT}=1.0 µF, R_L=150 Ω

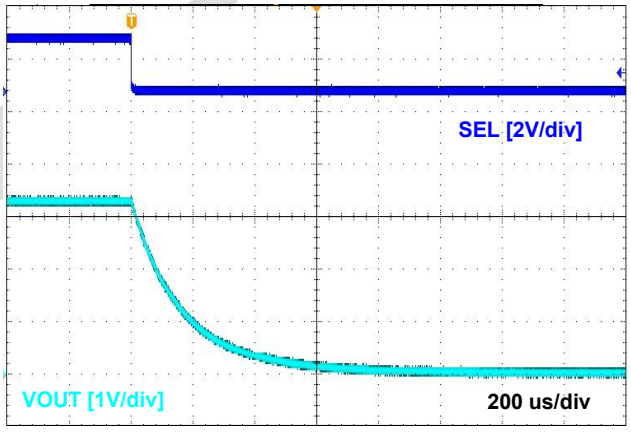


Figure 14. Turn-Off Response
V_{IN1}=3.3 V, C_{IN}=0.1 µF, C_{OUT}=1.0 µF, R_L=150 Ω

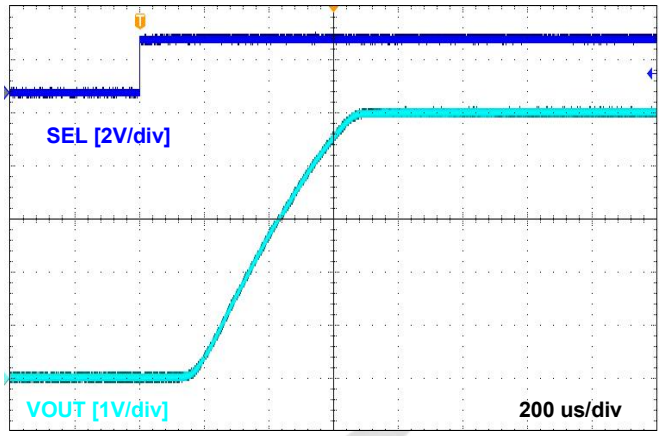


Fig Figure 15. Turn-On Response
V_{IN1}=5.0 V, C_{IN}=0.1 µF, C_{OUT}=1.0 µF, R_L=150 Ω

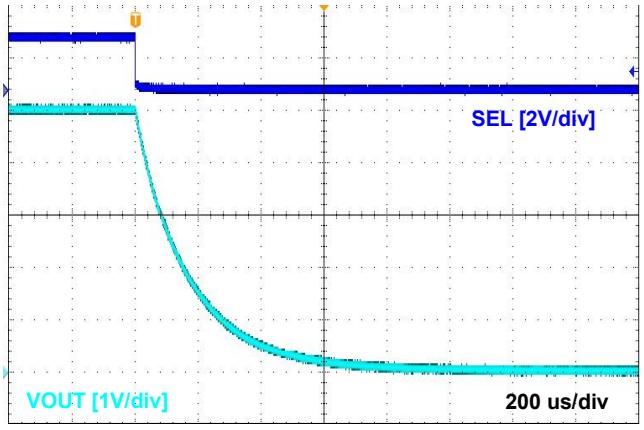


Figure 16. Turn-Off Response
V_{IN1}=5.0 V, C_{IN}=0.1 µF, C_{OUT}=1.0 µF, R_L=150 Ω

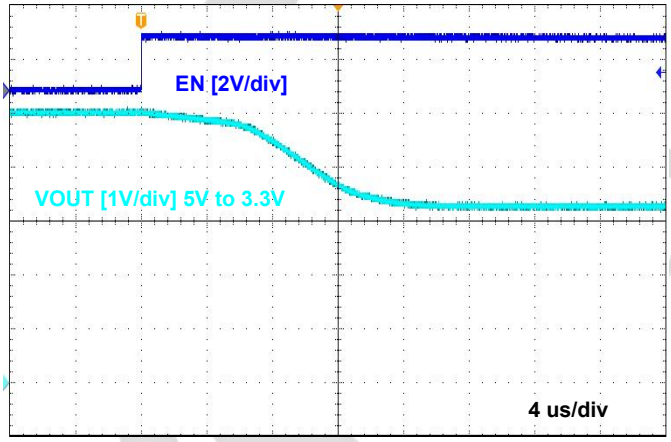


Figure 17. V_{OUT} Switchover from 5V to 3.3V
V_{IN1}=5.0 V, V_{IN2}=3.3 V C_{IN}=1.0 µF, C_{OUT}=1.0 µF, R_L=150 Ω

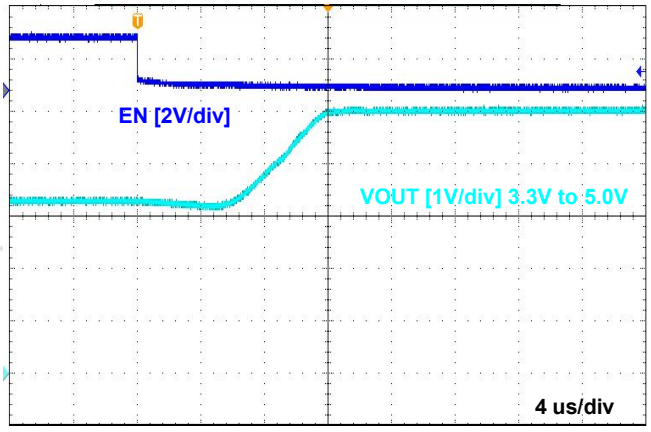


Figure 18. V_{OUT} Switchover from 3.3V to 5V
V_{IN1}=5.0 V, V_{IN2}=3.3 V C_{IN}=1.0 µF, C_{OUT}=1.0 µF, R_L=150 Ω

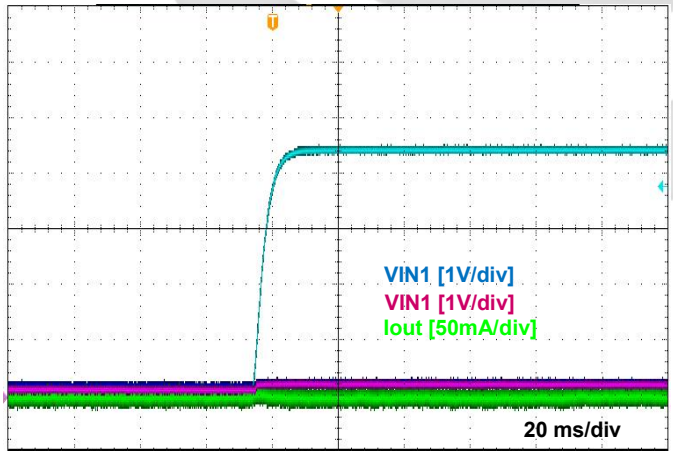


Figure 19. Reverse Current Blocking When Disabled
V_{IN1} = V_{IN2} =0 V, V_{OUT}=0 V to 4.5 V, C_{IN}=1.0 µF, C_{OUT}=1.0 µF, EN=SEL=0 V

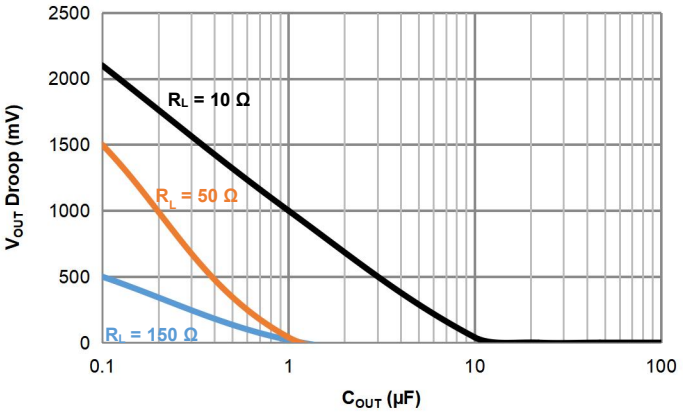


Figure 20. Output Voltage Droop at Switching Over from V_{IN1} (5V) to V_{IN2} (3V)

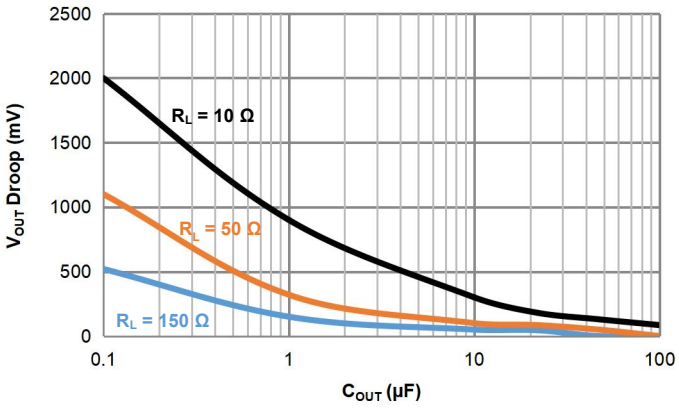


Figure 21. Output Voltage Droop at Switching Over from V_{IN2} (3V) to V_{IN1} (5V)

APPLICATION INFORMATION

The GLF74520 is a fully integrated 2.5 A Power Mux with a fixed slew rate control to limit the inrush current during device turn on. The GLF74520 also has a wide voltage operating range from 1.5 V to 5.5 V. In the off state, the GLF74520 consumes very low leakage current to avoid unwanted power drain from limited input power supplies. The GLF74520 utilizes a chip scale technology package with 6 bumps in a 0.97 mm x 1.47 mm x 0.55 mm package size with a 0.55 mm bump pitch.

Input Source Selection

By changing the state of the SEL and EN pins, the GLF74520 offers the automatic, as well as the manual input selection mode. In each mode, the V_{OUT} connects to one input source.

Input Capacitor

A capacitor is recommended to be placed close to the V_{IN} pin to reduce the voltage drop on the input power rail caused by transient inrush current at start-up. A higher input capacitor value can be used to further attenuate the input voltage drop.

Output Capacitor

An output capacitor is recommended to minimize voltage undershoot on the output pin during the transition when the switch is turned off. Undershoot can be caused by parasitic inductance from board traces or intentional load inductances. If load inductances do exist, use of an output capacitor can improve output voltage stability and system reliability. The C_{OUT} capacitor should be placed close to the V_{OUT} and GND pins.

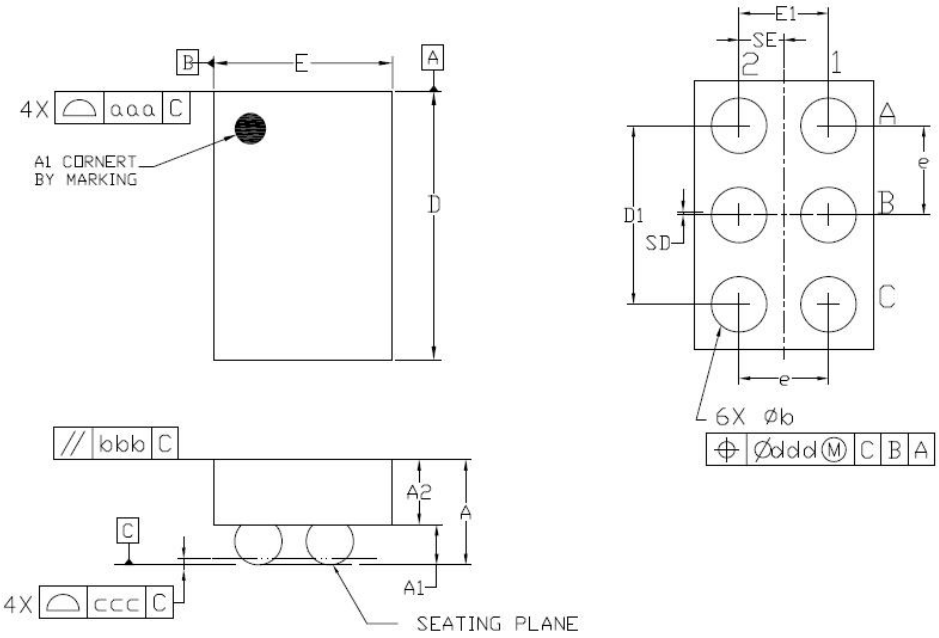
Reverse Current Blocking

The GLF74520 also prevents the reverse current from the output voltage when both switches are turned off at EN = SEL = 0 V.

Board Layout

All traces should be as short as possible to minimize parasitic inductance effect. Wide traces for V_{IN}, V_{OUT}, and GND will help reduce signal degradation and parasitic effects during dynamic operations as well as improve the thermal performance at high load current.

PACKAGE OUTLINE



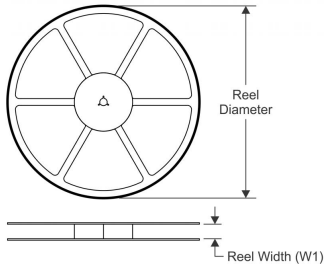
Dimensional Ref.			
REF.	Min.	Nom.	Max.
A	0.500	0.550	0.600
A1	0.225	0.250	0.275
A2	0.275	0.300	0.325
D	1.460	1.470	1.485
E	0.960	0.970	0.985
D1	0.950	1.000	1.050
E1	0.450	0.500	0.550
b	0.260	0.310	0.360
e	0.500 BSC		
SD	0.000 BSC		
SE	0.250 BSC		
Tol. of Form&Position			
aaa	0.10		
bbb	0.10		
ccc	0.05		
ddd	0.05		

Notes

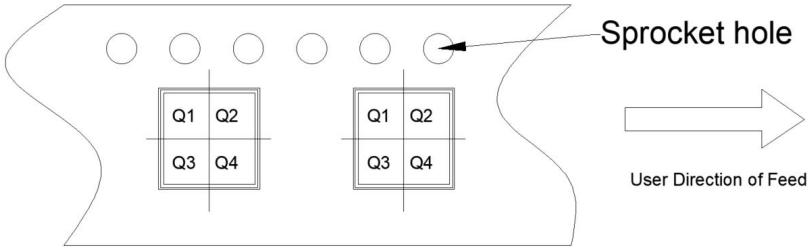
1. All DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.

TAPE AND REEL INFORMATION

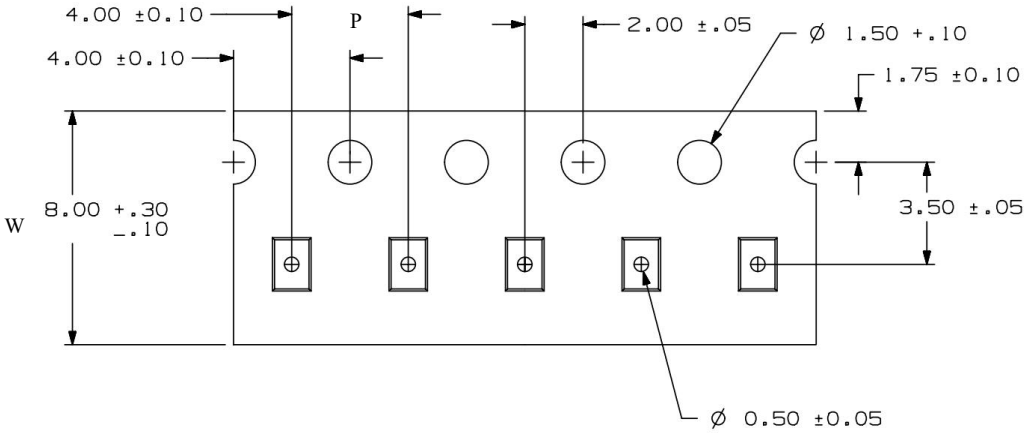
REEL DIMENSIONS

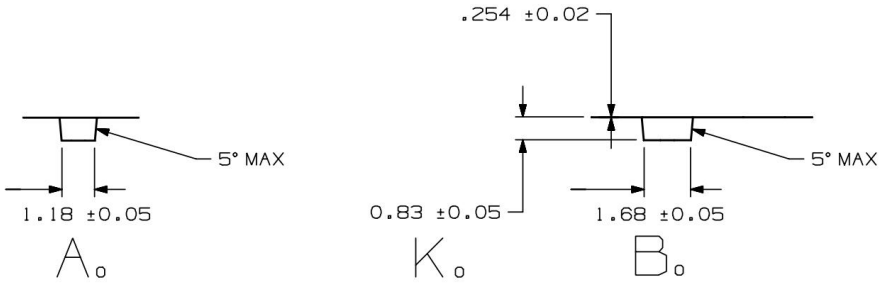


QUANRANT ASSIGNMENTS PIN 1 ORIENTATION TAPE



TAPE DIMENSIONS





Device	Package	Pins	SPQ	Reel Diameter(mm)	Reel Width W1	A0	B0	K0	P	W	Pin1
GLF74520	WLCSP	6	3000	180	9	1.18	1.68	0.83	4	8	Q1

Remark:

A0: Dimension designed to accommodate the component width

B0: Dimension designed to accommodate the component length

C0: Dimension designed to accommodate the component thickness

W: Overall width of the carrier tape

P: Pitch between successive cavity centers

SPECIFICATION DEFINITIONS

Document Type	Meaning	Product Status
Target Specification	This is a target specification intended to support exploration and discussion of critical needs for a proposed or target device. Spec limits including typical, minimum, and maximum values are desired, or target, limits. GLF reserves the right to change limits at any time without warning or notification. A target specification in no way guarantees future production of the device in question.	Design / Development
Preliminary Specification	This is a draft version of a product specification. The specification is still under internal review and subject to change. GLF reserves the right to change the specification at any time without warning or notification. A preliminary specification in no way guarantees future production of the device in question.	Qualification
Product Specification	This document represents the anticipated production performance characteristics of the device.	Production

DISCLAIMERS

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