

# 3 A, Ultra-low Power I<sub>Q</sub>Smart<sup>™</sup> Power Load Switch with True Reverse Current Blocking

**Product Specification** 

### DESCRIPTION

The GLF72110 / GLF72111 / GLF72112 is an advanced technology fully integrated I<sub>Q</sub>Smart<sup>™</sup> load switch device with True Reverse Current Blocking (TRCB) technology and slew rate control of the output voltage.

The GLF72110 / GLF72111 / GLF72112 offers industry leading True Reverse Current Blocking (TRCB) performance, featuring an ultra-low threshold voltage. It minimizes reverse current flow in the event that the VOUT pin voltage exceeds the VIN voltage.

The GLF72110 / GLF72111 / GLF72112 has industry leading efficiency. It features a  $R_{\text{ON}}$  as low as 29 m $\Omega$  typical at 5.5 V, reducing power loss during conduction. The device also features ultra-low shutdown current ( $I_{\text{SD}}$ ) to reduce power loss and battery drain in the off state. When EN is pulled low, and the output is grounded, the GLF72110 / GLF72111 / GLF72112 can achieve an  $I_{\text{SD}}$  as low as 24 nA typical at 5.5 V.

The GLF72110 / GLF72111 / GLF72112 load switch device supports an industry leading wide input voltage range and helps to improve operating life and system robustness. Furthermore, one device can be used in multiple voltage rail applications which helps to simplify inventory management and reduces operating cost.

The GLF72110 / GLF72111 / GLF72112 load switch device is small, utilizing a chip scale package with 4 bumps in a 0.97 mm x 0.97 mm x 0.55 mm die size and a 0.5 mm pitch.

### **FEATURES**

• True Reverse Current Blocking

 $\bullet$  Ultra-Low Iq: 1.3  $\mu A$  Typ at 5.5  $V_{IN}$ 

• Ultra-Low I<sub>SD</sub>: 24 nA Typ at 5.5 V<sub>IN</sub>

• Low  $R_{ON}$ : 29 m $\Omega$  Typ at 5.5 $V_{IN}$ 

• I<sub>OUT</sub> Max: 3 A

• Wide Input Range: 1.5 V to 5.5 V

6 V<sub>ABS</sub> max

Controlled Rise Time

• Internal EN Pull-Down Resistor, REN

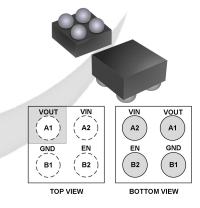
 Integrated Output Discharge Switch: GLF72111

 0.97 mm x 0.97 mm x 0.55 mm Wafer Level Chip Scale Package

## **APPLICATIONS**

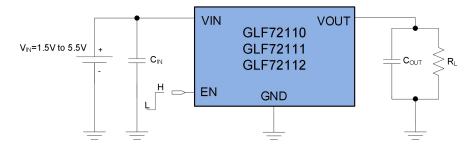
- Mobile Devices
- Wearables
- Low Power Subsystems

## **PACKAGE**



0.97 mm x 0.97 mm x 0.55 mm WLCSP

# **APPLICATION DIAGRAM**



# **ALTERNATE DEVICE OPTIONS**

Part Number	Top Mark	R <sub>ON</sub> (Typ) at 5.5 V	Rise Time t <sub>R</sub> (µs) at 3.3 V	Output Discharge	EN Activity
GLF72110	DC		1200	NA	
GLF72111	BJ	29 mΩ	1200	85 Ω	High
GLF72112	KC		18	NA	

# **FUNCTIONAL BLOCK DIAGRAM**

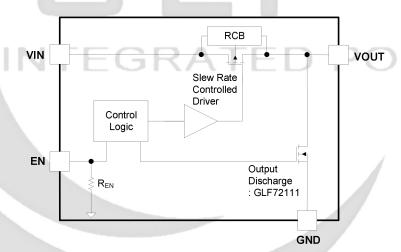


Figure 1. Functional Block Diagram

# PIN CONFIGURATION

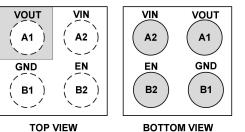


Figure 2. 0.97mm x 0.97mm x 0.55mm WLCSP

# **PIN DEFINITION**

Pin#	Name	Description
A1	V <sub>оит</sub>	Switch Output
A2	Vin	Switch Input. Supply Voltage for IC
B1	GND	Ground
B2	EN	Enable to control the switch. It has an internal 10 $M\Omega$ pull down resistor, $R_{\text{EN}}.$

# **ABSOLUTE MAXIMUM RATINGS (1)**

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions; extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Pa	rameter	Min.	Max.	Unit
V <sub>IN</sub>	V <sub>IN</sub> , V <sub>OUT</sub> , V <sub>EN</sub> to GND			6	V
	Maximum Continuous Switch Current a		3	٨	
l <sub>out</sub>	Maximum Continuous Switch Current a		2	Α	
P <sub>D</sub>	Power Dissipation at T <sub>A</sub> = 25 °C			1.2	W
TJ	Maximum Junction Temperature			150	°C
T <sub>STG</sub>	Storage Junction Temperature			150	°C
T <sub>A</sub>	Ambient Operating Temperature Range	;	-40	125	°C
θ <sub>JA</sub> <sup>(2)</sup>	Thermal Resistance, Junction to Ambient			85	°C/W
ESD	Floatrostatic Discharge Canability	Human Body Model, JESD22-A114			14) /
EOD	Electrostatic Discharge Capability	Charged Device Model, JESD22-C101	2		kV

- Continuous operation even under Absolute Maximum Ratings may cause this device serious reliability problems.
  The thermal resistance depends on the PCB conditions for heat dissipation. All pins are strongly recommended to have a solid contact to larger Cu layer areas

# RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Max.	Unit
V <sub>IN</sub>	Supply Voltage	1.5	5.5	V
T <sub>A</sub>	Ambient Operating Temperature	- 40	+125	°C

# **ELECTRICAL CHARACTERISTICS**

Values are at  $V_{IN}$  = 3.3 V and  $T_A$  = 25 °C unless otherwise noted.

Symbol	Parameter	Conditions			Тур.	Max.	Units
Basic Ope	eration						
		EN = Enable, I <sub>OUT</sub> =0 mA, V <sub>IN</sub> = V <sub>EN</sub> =5.5 V			1.3	2.0	μА
IQ	Quiescent Current (1)	EN=Enable, I <sub>OUT</sub> =0 mA, V <sub>IN</sub> =V <sub>EN</sub> =5.5 V, T <sub>A</sub> =85 °C <sup>(5)</sup>			1.4		
		EN=Enable, I <sub>OUT</sub> =0 mA, V <sub>IN</sub> =V <sub>EN</sub> =5.5 V, T <sub>A</sub> =125 °C <sup>(5)</sup>			1.5		1
		EN = Disable, I <sub>OUT</sub> =0 mA, V <sub>IN</sub> =1.5 V					
		EN = Disable, I <sub>OUT</sub> =0 mA, V <sub>I</sub>	<sub>N</sub> =3.3 V		5	30	]
	Charteless Comment	EN = Disable, I <sub>OUT</sub> =0 mA, V <sub>I</sub>	<sub>N</sub> =4.2 V		12		- nA
I <sub>SD</sub>	Shutdown Current	EN = Disable, I <sub>OUT</sub> =0 mA, V <sub>I</sub>	<sub>N</sub> =5.5 V		24	50	1
		EN = Disable, I <sub>OUT</sub> =0 mA, V <sub>I</sub>	<sub>N</sub> =5.5 V, T <sub>A</sub> =85 °C <sup>(5)</sup>		0.5		
		EN = Disable, I <sub>OUT</sub> =0 mA, V <sub>I</sub>	<sub>N</sub> =5.5 V, T <sub>A</sub> =125 °C <sup>(5)</sup>		4.4		μA
			T <sub>A</sub> =25 °C		29	34	
R <sub>on</sub> (	On-Resistance	V <sub>IN</sub> =5.5 V, I <sub>OUT</sub> = 500 mA	T <sub>A</sub> =85 °C <sup>(5)</sup>		32		mΩ
			T <sub>A</sub> =125 °C <sup>(5)</sup>		35		
			T <sub>A</sub> =25 °C		35	41	
		V <sub>IN</sub> =3.3 V, I <sub>OUT</sub> = 500 mA	T <sub>A</sub> =85 °C <sup>(5)</sup>		40		
A		EGRAT	T <sub>A</sub> =125 °C <sup>(5)</sup>	DV	44	- F	
		V <sub>IN</sub> =1.8 V, I <sub>OUT</sub> = 300 mA	T <sub>A</sub> =25 °C		54		
		V <sub>IN</sub> =1.5 V, I <sub>OUT</sub> = 100 mA	T <sub>A</sub> =25 °C		66		
R <sub>DSC</sub>	Output Discharge Resistance, GLF72111	E <sub>N</sub> =Low, I <sub>FORCE</sub> = 10 mA		70	85	100	Ω
VIH	EN Input Logic High Voltage	V <sub>IN</sub> =1.5 V to 5.5 V		1.2			\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
VIL	EN Input Logic Low Voltage	V <sub>IN</sub> =1.5 V to 5.5 V				0.4	\ \ \
R <sub>EN</sub>	EN pull down resistance	Internal Resistance			10		ΜΩ
I <sub>EN</sub>	EN Source or Sink Current	E <sub>N</sub> =V <sub>IN</sub> or GND				0.6	μΑ
V <sub>RCB_TH</sub>	RCB Protection Threshold Voltage	Vout - Vin			28		
V <sub>RCB_RL</sub>	RCB Protection Release Voltage	V <sub>IN</sub> - V <sub>OUT</sub>			28		mV
Switching	Characteristics (4), (5) : GLF72	110, GLF72111			•	•	
t <sub>dON</sub>	Turn-On Delay (2)	3.3 V <sub>IN</sub> , R <sub>I</sub> =150, O, C <sub>OUT</sub> =0.1 µF		0.75	1.0	1.25	
t <sub>R</sub>	V <sub>OUT</sub> Rise Time <sup>(2)</sup>			0.9	1.2	1.5	ms
t <sub>dOFF</sub>	Turn-Off Delay (3)	0.01/ D. 450.00	4E. OLEZO440		1.8		
t <sub>F</sub>	V <sub>OUT</sub> Fall Time <sup>(3)</sup>	3.3 $V_{IN}$ , $R_L$ =150 Ω, $C_{OUT}$ =0.	1 μr, GLF/2110		29		1
t <sub>dOFF</sub>	Turn-Off Delay (3)	0.01/ D. 450.0.0	4		0.9		μs
t <sub>F</sub>	V <sub>OUT</sub> Fall Time <sup>(3)</sup>	3.3 $V_{IN}$ , $R_L$ =150 $\Omega$ , $C_{OUT}$ =0.1 $\mu$ F, GLF72111			15		1

Switchin	g Characteristics (4), (5): GLF72	1112		
$t_{dON}$	Turn-On Delay (2)		15	
t <sub>R</sub>	V <sub>OUT</sub> Rise Time (2)	0.01/ 5.450.0.0.0.4.5	18	
t <sub>dOFF</sub>	Turn-Off Delay (3)	3.3 V <sub>IN</sub> , R <sub>L</sub> =150 Ω, C <sub>OUT</sub> =0.1 μF	1.8	
t <sub>F</sub>	V <sub>OUT</sub> Fall Time <sup>(3)</sup>		29	
$t_{dON}$	Turn-On Delay (2)		5	μs
t <sub>R</sub>	V <sub>OUT</sub> Rise Time <sup>(2)</sup>		9	
t <sub>dOFF</sub>	Turn-Off Delay (3)	5.5 V <sub>IN</sub> , R <sub>L</sub> =150 Ω, C <sub>OUT</sub> =0.1 μF	1.5	
t <sub>F</sub>	V <sub>OUT</sub> Fall Time (3)		32	

Notes:

- 1.  $I_Q$  does NOT include Enable pull down current through the pull down resistor  $R_{PD}$ .
- 2.  $t_{ON} = t_{dON} + t_{R}$
- 3.  $t_{OFF} = t_{dOFF} + t_F$
- Output discharge path is enabled during off.
  By design; characterized, not production tested.

# **TIMING DIAGRAM**

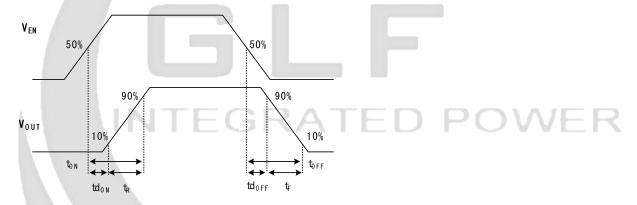


Figure 3. Timing Diagram

# TYPICAL PERFORMANCE CHARACTERISTICS

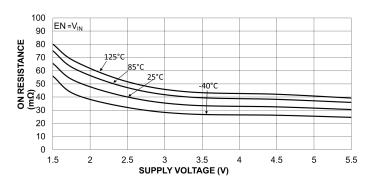


Figure 4. On-Resistance vs. Supply Voltage

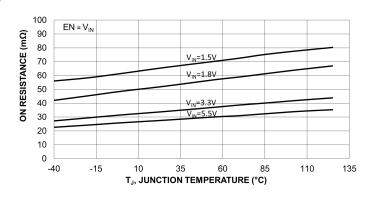


Figure 5. On-Resistance vs. Temperature

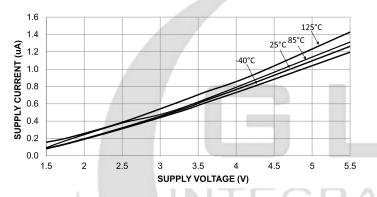


Figure 6. Quiescent Current vs. Supply Voltage

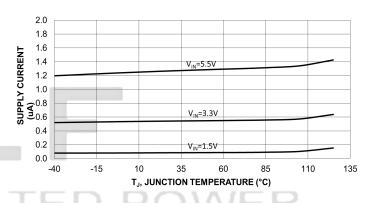


Figure 7. Quiescent Current vs. Temperature

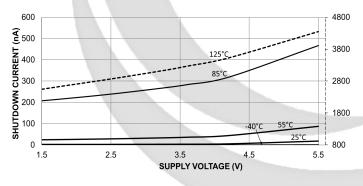


Figure 8. Shutdown Current vs. Supply Voltage

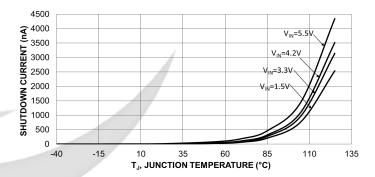
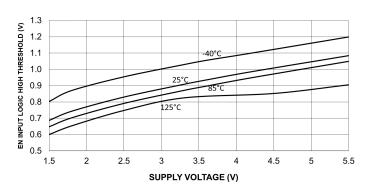


Figure 9. Shutdown Current vs. Temperature

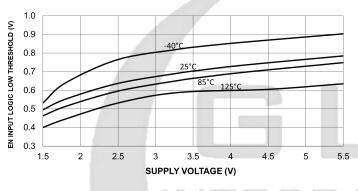




1.3 EN INPUT LOGIC HIGH THRESHOLD(V) 1.2 V<sub>IN</sub>=5.5V 1.1 1.0 V<sub>IN</sub>=3.3V 0.9 8.0 V<sub>IN</sub>=1.5V 0.7 0.6 0.5 0.4 -40 -15 10 35 60 85 110 135 T<sub>J</sub>, JUNCTION TEMPERATURE (°C)

Figure 10. EN Input Logic High Threshold

Figure 11. EN Input Logic High Threshold Vs. Temperature



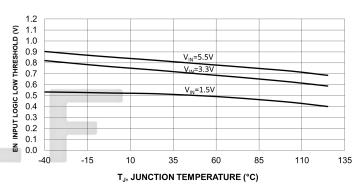
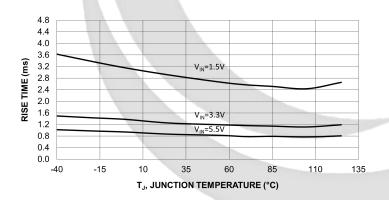


Figure 12. EN Input Logic Low Threshold

Figure 13. EN Input Logic Low Threshold Vs. Temperature



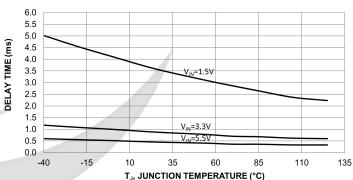
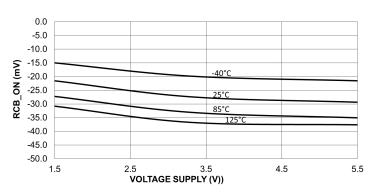


Figure 14. Vout Rise Time vs. Temperature GLF72110 and GLF72111

Figure 15. Turn-On Delay Time vs. Temperature GLF72110 and GLF72111

# 3 A, Ultra-low Power IoSmart™ Power Load Switch with TRCB



0.0 -5.0 -10.0 -15.0 -20.0 -25.0 -30.0 -35.0 -40.0

Figure 16. RCB Threshold Voltage vs. Supply Voltage

Figure 17. RCB Threshold Voltage vs. Temperature

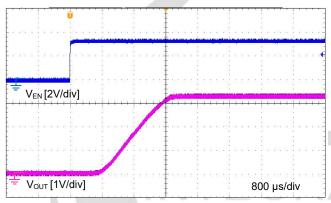


Figure 18. Turn-On Response, GLF72110  $V_{IN}$ =3.3 V,  $C_{IN}$ =0.1  $\mu$ F,  $C_{OUT}$ =0.1  $\mu$ F,  $R_L$ =150  $\Omega$ 

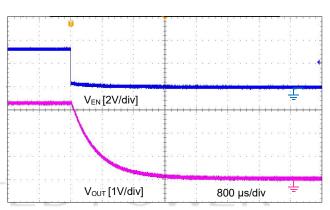


Figure 19. Turn-Off Response, GLF72110  $V_{\text{IN}}{=}3.3$  V,  $C_{\text{IN}}{=}0.1~\mu\text{F},~C_{\text{OUT}}{=}0.1~\mu\text{F},~R_{\text{L}}{=}150~\Omega$ 

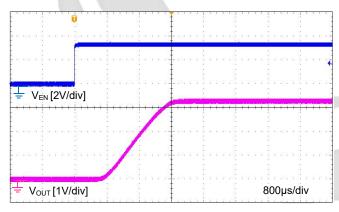


Figure 20. Turn-On Response, GLF72111  $V_{\text{IN}}{=}3.3~V,~C_{\text{IN}}{=}0.1~\mu\text{F},~C_{\text{OUT}}{=}0.1~\mu\text{F},~R_{\text{L}}{=}150~\Omega$ 

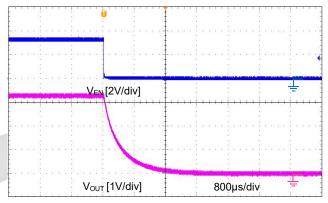


Figure 21. Turn-Off Response, GLF72111  $V_{\text{IN}}{=}3.3~V,~C_{\text{IN}}{=}0.1~\mu\text{F},~C_{\text{OUT}}{=}0.1~\mu\text{F},~R_{\text{L}}{=}150~\Omega$ 

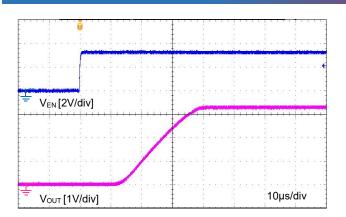


Figure 22. Turn-On Response, GLF72112  $V_{IN}$ =3.3 V,  $C_{IN}$ =0.1  $\mu$ F,  $C_{OUT}$ =0.1  $\mu$ F,  $R_L$ =150  $\Omega$ 

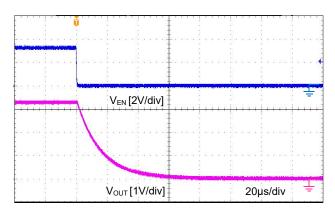


Figure 23. Turn-Off Response, GLF72112  $V_{IN}$ =3.3 V,  $C_{IN}$ =0.1  $\mu$ F,  $C_{OUT}$ =0.1  $\mu$ F,  $R_L$ =150  $\Omega$ 

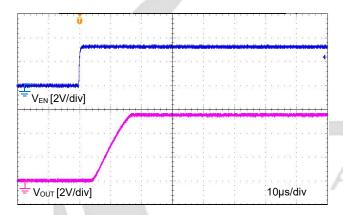


Figure 24. Turn-On Response, GLF72112  $V_{IN}=5.5 \text{ V}, C_{IN}=0.1 \mu\text{F}, C_{OUT}=0.1 \mu\text{F}, R_L=150 \Omega$ 

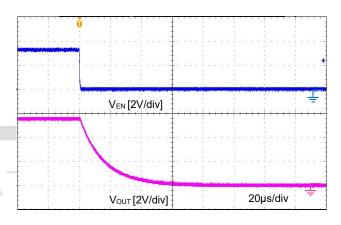


Figure 25. Turn-Off Response, GLF72112  $V_{IN}=5.5 \text{ V}, C_{IN}=0.1 \mu\text{F}, C_{OUT}=0.1 \mu\text{F}, R_L=150 \Omega$ 

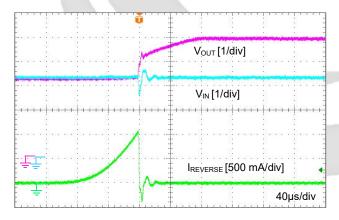


Figure 26. Reverse Current Blocking at Switch On  $V_{IN} = 3.3 \text{ V}, V_{OUT} = \text{From } 3.3 \text{ V to } 4 \text{ V}, C_{IN} = 0.1 \mu\text{F}, C_{OUT} = 0.1 \mu\text{F}$ 



3 A, Ultra-low Power IoSmart™ Power Load Switch with TRCB

### APPLICATION INFORMATION

The GLF72110, GLF72111 and GLF72112 are an integrated 3 A, Ultra-Efficient  $I_QSmart^{TM}$  Load Switch device with a fixed slew rate control to limit the inrush current during turn on. Each device is capable of operating over a wide input range from 1.5 V to 5.5 V with very low on-resistance to reduce conduction losses. In the off state, these devices consume very low leakage current to avoid unwanted standby current and save limited input power. The package is a 0.97 mm x 0.97 mm x 0.55 mm wafer level chip scale package, saving space in compact applications. It is constructed using 4 bumps, with a 0.5 mm pitch for manufacturability.

### Input and Output Capacitor

The GLF72110, GLF72111 and GLF72112 require an input capacitor to function. To reduce a voltage drop on the input power rail caused by transient inrush current at start-up, a 0.1  $\mu$ F capacitor is recommended to be placed close to  $V_{IN}$  pin. A higher input capacitor value can be used to attenuate the input voltage drop. In addition, a 0.1  $\mu$ F capacitor or higher can be also used to prevent undershoot caused by parasitic inductance on board traces and improve reliability of a controlled voltage rail. The  $C_{OUT}$  should be placed close to VOUT and GND pins.

## EN pin

The GLF72110, GLF72111 and GLF72112 can be activated by forcing the EN pin to a high level. Note that the EN pin has an internal pull-down resistor to help pull the main switch to a known "off state" when no EN signal is applied from an external controller.

# True Reverse Current Blocking

The GLF72110, GLF72111 and GLF72112 have a built-in reverse current blocking protection which always monitors the output voltage level regardless of the status of EN pin to check if it is greater than the input voltage. When the output voltage goes beyond the input voltage by 28 mV, that is the reverse current blocking protection trip voltage, the reverse current blocking function block turns off the switch. Note that some reverse current can occur until the  $V_{RCB}$  is triggered. The main switch will resume normal operation when the output voltage drops below the input source by the RCB protection release voltage.

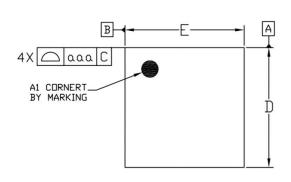
# **Output Discharge Function**

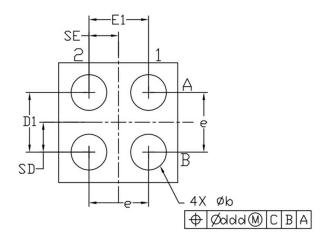
The GLF72111 has an internal discharge N-channel FET switch on the VOUT pin. When EN signal turns the main power FET to an off state, the N-channel switch turns on to discharge an output capacitor guickly.

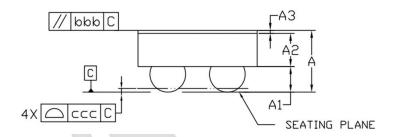
### **Board Layout**

All traces should be as short as possible to minimize parasitic inductance effects. Wide traces for VIN, VOUT, and GND will help reduce signal degradation and parasitic effects during dynamic operation as well as improve the thermal performance at high load current.

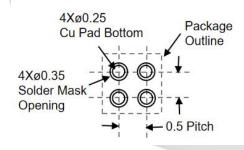
# **PACKAGE OUTLINE**







# **Recommended Footprint**



D:	2010221	D - 6
ulme	nsional	ReT.

REF.	Min.	Nom.	Max.				
Α	0.500	0.550	0.600				
A1	0.225	0.250	0.275				
A2	0.255	0.275	0.300				
Α3	0.020	0.025	0.030				
D	0.960	0.970	0.985				
Ε	0.960	0.970	0.985				
D1	0.450	0.500	0.550				
E1	0.450	0.500	0.550				
Ь	0.260	0.310	0.360				
е	0	.500 BSC					
SD	0	.250 BS	C				
SE	0	.250 BS	C				
To	ol. of Fo	ol. of Form&Position					
aaa	0.10						
bbb	0.10						
ccc		0.05					
ddd		0.05					

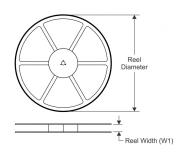
#### Notes

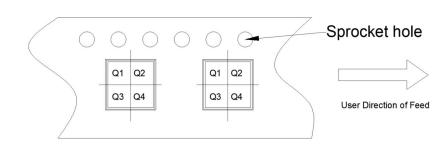
- 1. ALL DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGRESS)
- 2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.
- 3. A3: BACKSIDE LAMINATION

# TAPE AND REEL INFORMATION

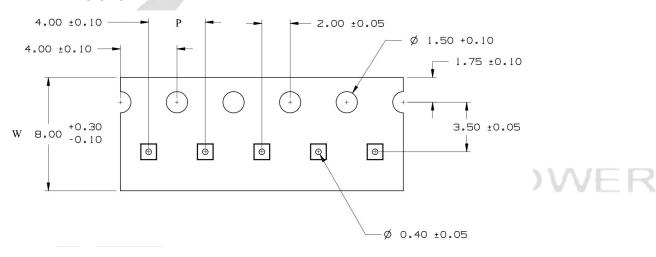
# **REEL DIMENSIONS**

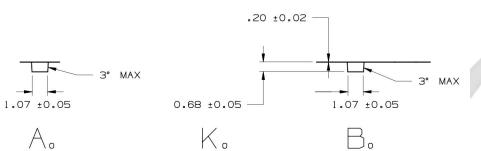
# **QUADRANT ASSIGNMENTS PIN 1 ORIENTATION TAPE**





### TAPE DIMENSIONS





Device	Package	Pins	SPQ	Reel Diameter(mm)	Reel Width W1	A0	В0	K0	Р	w	Pin1
GLF72110	WLCSP	4	3000	180	9	1.07	1.07	0.68	4	8	Q1
GLF72111	WLCSP	4	3000	180	9	1.07	1.07	0.68	4	8	Q1
GLF72112	WLCSP	4	3000	180	9	1.07	1.07	0.68	4	8	Q1

#### Remark:

- A0: Dimension designed to accommodate the component width
- B0: Dimension designed to accommodate the component length
- C0: Dimension designed to accommodate the component thickness
- Overall width of the carrier tape
- Pitch between successive cavity centers



3 A, Ultra-low Power IoSmart™ Power Load Switch with TRCB

# **SPECIFICATION DEFINITIONS**

Document Type	Meaning	Product Status
Target Specification	This is a target specification intended to support exploration and discussion of critical needs for a proposed or target device. Spec limits including typical, minimum, and maximum values are desired, or target, limits. GLF reserves the right to change limits at any time without warning or notification. A target specification in no way guarantees future production of the device in question.	Design / Development
Preliminary Specification	This is a draft version of a product specification. The specification is still under internal review and subject to change. GLF reserves the right to change the specification at any time without warning or notification. A preliminary specification in no way guarantees future production of the device in question.	Qualification
Product Specification	This document represents the anticipated production performance characteristics of the device.	Production

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