

DESCRIPTION

The GLF4020 is an integrated power multiplexer switch with dual independent power switches connected to a single output pin to enable seamless transition between two input sources.

The GLF4020 provides an automatic selection mode as well as a manual selection mode by the combination of the logic input pins of EN and SEL. The EN input pin is used along with the select (SEL) input pin to select the automatic switching function, select VIN1 only, select VIN2 only, or turn both switches off. In the automatic selection mode, the GLF4020 automatically selects the higher input voltage source out of two input DC power supplies.

The GLF4020 features an ultra-efficient I_{QSmart}^{TM} technology that offers quiescent current (I_Q) and shutdown current (I_{SD}) in the industry. Low R_{ON} reduces conduction losses while low I_Q and I_{SD} solutions help designers to reduce parasitic leakage current, improve system efficiency, and increase battery lifetime.

The GLF4020 blocks any cross-conduction current between two input power sources. When the switch is disabled, the GLF4020 prevents the reverse current to the input source from the output at any higher V_{out} than V_{in} condition.

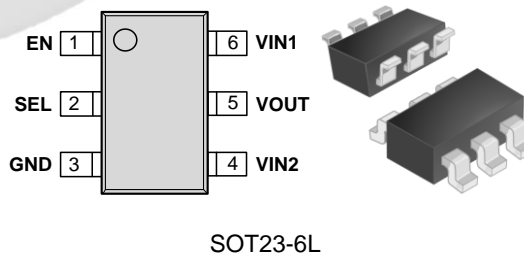
FEATURES

- Two-Input and Single-Output Power Multiplexer Switch
- Automatic and Manual Input Selection Mode
- Supply Voltage Range: 2.5 V to 6.5 V
7.0 V_{Abs} Max
- R_{ON} : 92 m Ω Typ. at 6.5 V_{IN1} or V_{IN2}
105 m Ω Typ. at 4.5 V_{IN1} or V_{IN2}
- 2 A Continuous Output Current Capability Per Channel
- Ultra-Low Supply Current at Operation
 I_Q : 4 μ A Typ at 6.5 V_{IN}
- Ultra-Low Stand-by Current
 I_{SD} : 6 nA Typ at 6.5 V_{IN}
- Smart Control Pins
 I_{EN} and I_{SEL} : 3 nA Typ at V_{EN} or V_{SEL} > V_{IH}
 R_{EN} and R_{SEL} : 500 k Ω Typ
- No Cross Conduction Between Two Inputs
- Reverse Current Blocking when Disabled
- Operating Temperature Range: -40 °C to 85 °C
- HBM: 6 kV, CDM: 2 kV

APPLICATIONS

- Smart Devices
- Smart Home Electronics

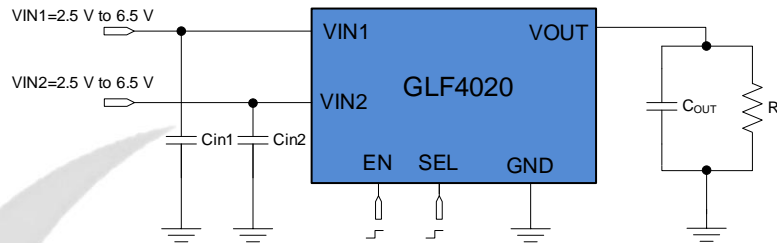
PACKAGE



DEVICE ORDERING INFORMATION

Part Number	Top Mark	R _{ON} at 6.5 V _{IN}	Output Current, I _{OUT}	Ultra-low I _Q at 6.5 V _{IN}
GLF4020-T2G7	DP	92 mΩ	2 A	4 μA

APPLICATION DIAGRAM



FUNCTIONAL BLOCK DIAGRAM

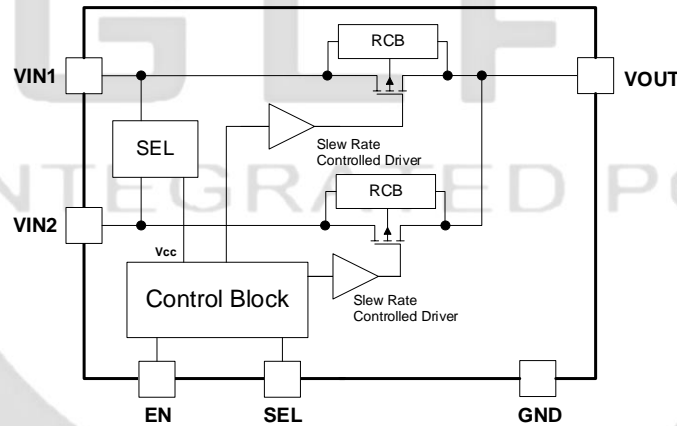


Figure 1. Functional Block Diagram

PIN CONFIGURATION

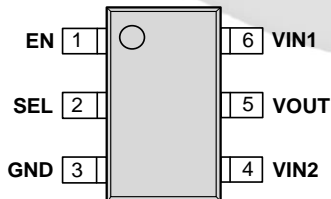


Figure 2. SOT23-6L

PIN DEFINITION

Pin #	Name	Description
1	EN	Enable to control the switch. Do not leave the EN pin floating.
2	SEL	Input Source Selection. Do not leave the SEL pin floating.
3	GND	Ground
4	VIN2	Switch Input 2
5	VOUT	Switch Output
6	VIN1	Switch Input 1

ABSOLUTE MAXIMUM RATINGS

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions; extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
VIN1, VIN2 VOUT, EN	Each Pin Voltage Range to GND		-0.3	7.0	V
I _{OUT}	Maximum Continuous Switch Current			2.0	A
P _D	Power Dissipation at T _A = 25°C			1.0	W
T _{STG}	Storage Junction Temperature		-65	150	°C
T _A	Operating Temperature Range		-40	85	°C
θ _{JC}	Thermal Resistance, Junction to Case			90	°C/W
θ _{JA}	Thermal Resistance, Junction to Ambient			180	°C/W
ESD	Electrostatic Discharge Capability	Human Body Model, JESD22-A114	6		kV
		Charged Device Model, JESD22-C101	2		

Notes: 1. The thermal resistance depends on the PCB layout and heat dissipation.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Max.	Unit
VIN1, VIN2	Supply Voltage	2.5	6.5	V
T _A	Ambient Operating Temperature	-40	+85	°C

ELECTRICAL CHARACTERISTICS

$V_{IN1} = V_{IN2} = 2.5 \text{ V to } 6.5 \text{ V}$ and $T_A = 25^\circ\text{C}$. Unless otherwise noted

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	
Basic Operation							
I _{Q1} , I _{Q2}	Quiescent Current	V _{IN1} = 6.5 V, V _{IN2} < V _{in1} , I _{OUT} = 0 mA, EN = 0 V, SEL = V _{IN1} , V _{OUT} = V _{IN1} or V _{IN2} = 6.5 V, V _{IN1} < V _{IN2} , I _{OUT} = 0 mA, EN = SEL = V _{IN2} , V _{OUT} = V _{IN2}		4	5.5	μA	
		As above, Ta = 85°C ⁽¹⁾		5			
		I _{SD1} , I _{SD2}	Shutdown Current	V _{IN1,2} = 6.5 V, V _{OUT} = GND, EN = SEL = 0 V		6	20
V _{IN1,2} = 6.5 V, V _{OUT} = GND, EN = SEL = 0 V, Ta=85 °C ⁽¹⁾				60			
R _{ON}	On-Resistance	V _{IN1} or V _{IN2} = 6.5 V I _{OUT} = 500 mA	Ta = 25 °C		92	98	mΩ
			Ta = 85 °C ⁽¹⁾		110		
		V _{IN1} or V _{IN2} = 5.5 V, I _{OUT} = 500 mA	Ta = 25 °C		97	107	
			Ta = 85 °C ⁽¹⁾		115		
		V _{IN1} or V _{IN2} = 4.5 V, I _{OUT} = 500 mA	Ta = 25 °C		105	118	
			Ta = 85 °C ⁽¹⁾		125		
		V _{IN1} or V _{IN2} = 3.3 V, I _{OUT} = 300 mA	Ta = 25 °C		120	135	
		V _{IN1} or V _{IN2} = 2.5 V, I _{OUT} = 100 mA	Ta = 25 °C		145	162	
V _{IH}	EN, SEL Input Logic High Voltage		1.2			V	
V _{IL}	EN, SEL Input Logic Low Voltage				0.4	V	
I _{EN} , I _{SEL}	EN, SEL Current	V _{EN} or V _{SEL} > V _{IH} , Enabled		3	20	nA	
R _{EN} , R _{SEL} ⁽¹⁾	EN, SEL Pulldown Resistance	V _{EN} or V _{SEL} < V _{IL} , Disabled		500		kΩ	
I _{RVS}	Reverse Current ⁽¹⁾	V _{IN1} = V _{IN2} =0 V, V _{OUT} =5.5 V, EN=SEL=0 V		2.5		μA	
Switching Characteristics ⁽²⁾							
t _{dON}	Turn-On Delay	V _{IN1} = 6.5 V, V _{IN2} = 4.5 V R _L =150 Ω, C _{OUT} =1.0 μF		300		μs	
t _R	V _{OUT} Rise Time			448			
T _{dHL}	High-low Delay ⁽¹⁾			6			
T _{fHL}	High-low Fall Time ⁽¹⁾			4			
V _{droop}	Voltage Droop ⁽¹⁾			160		mV	
T _{dLH}	Low-high Delay ⁽¹⁾			11		μs	
Tr _{LH}	Low-high Rise Time ⁽¹⁾			4			
t _{dOFF}	Turn-Off Delay ⁽¹⁾			13			
t _F	V _{OUT} Fall Time ⁽¹⁾			350			

Notes:

1. By design; characterized, not production tested.
2. $t_{ON} = t_{dON} + t_R$, $t_{OFF} = t_{dOFF} + t_F$

TIMING DIAGRAM AND TRUTH TABLE

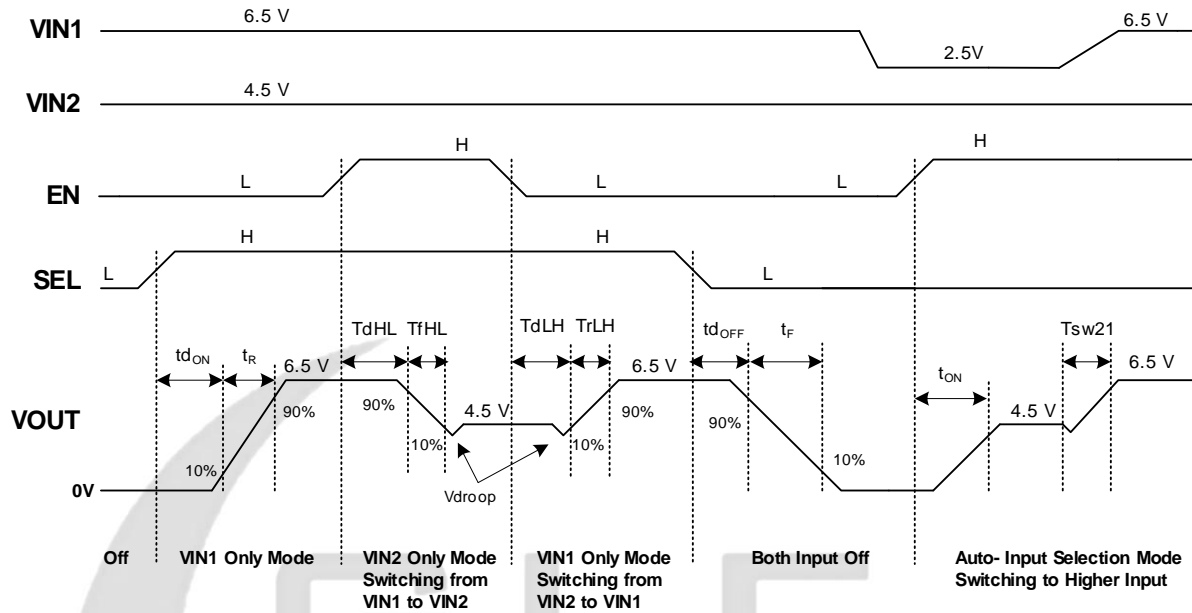


Figure 3. Timing Diagram

SEL	EN	Function	VOUT
0	0	Both switches are off	High-Z
0	1	Auto-Input selection. Vout is connected to a higher input source automatically	Higher Input between VIN1 and VIN2
1	0	Only VIN1 is selected	VIN1
1	1	Only VIN2 is selected	VIN2

Table 1. Truth Table of Input Source Selection

TYPICAL PERFORMANCE CHARACTERISTICS

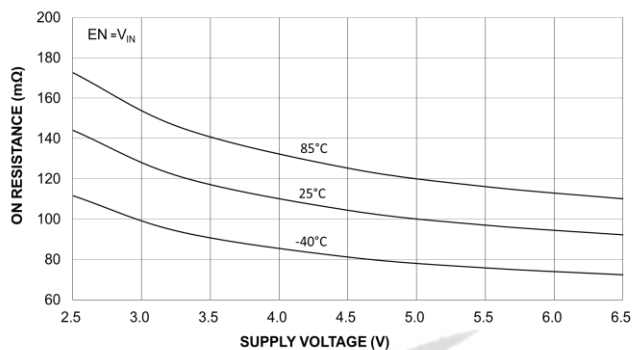


Figure 4. On-Resistance vs. Supply Voltage

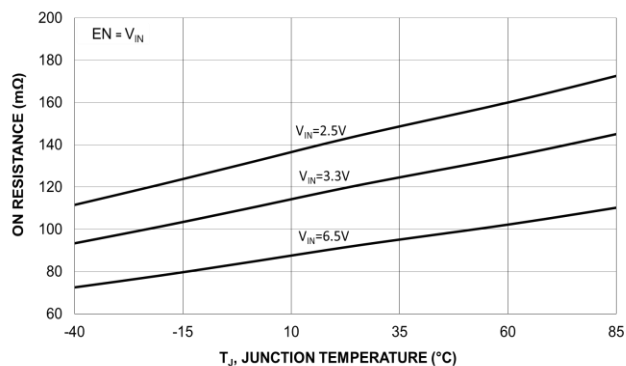


Figure 5. On-Resistance vs. Temperature

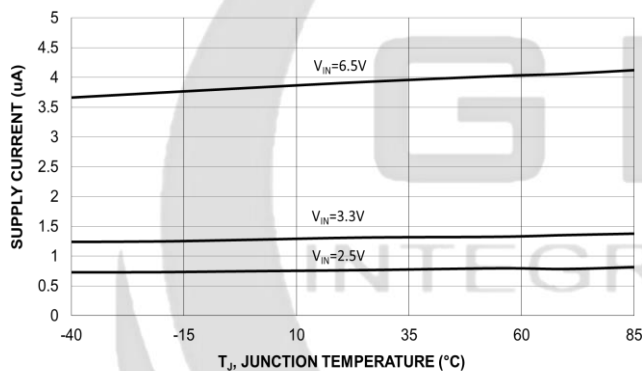


Figure 6. Quiescent Current vs. Temperature

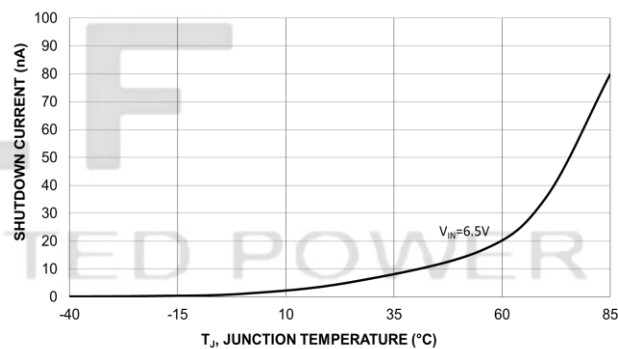


Figure 7. Shutdown Current vs. Temperature

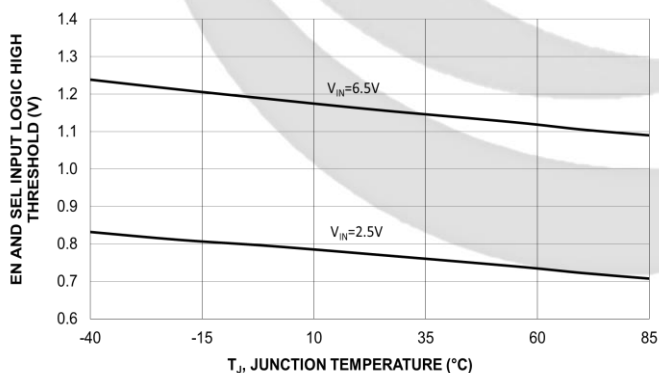


Figure 8. EN and SEL Input Logic High Threshold Vs. Temperature

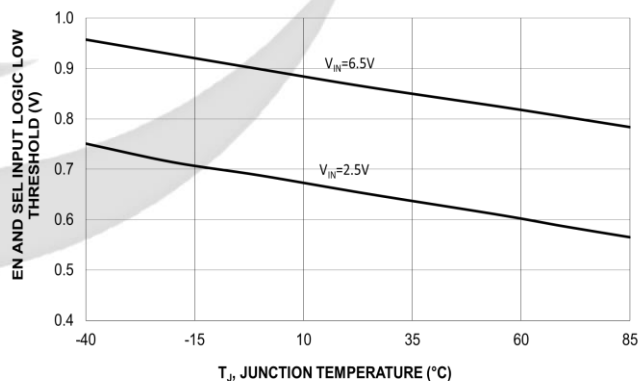


Figure 9. EN and SEL Input Logic Low Threshold Vs. Temperature

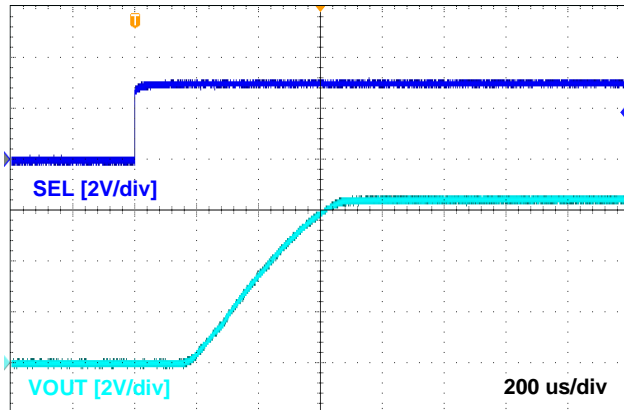


Figure 10. Turn-On Response
 $V_{IN1}=6.5\text{ V}$, $C_{IN}=0.1\text{ }\mu\text{F}$, $C_{OUT}=1.0\text{ }\mu\text{F}$, $R_L=150\text{ }\Omega$

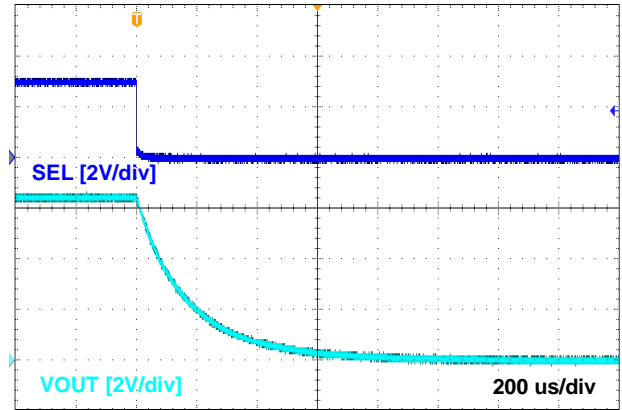


Figure 11. Turn-Off Response
 $V_{IN1}=6.5\text{ V}$, $C_{IN}=0.1\text{ }\mu\text{F}$, $C_{OUT}=1.0\text{ }\mu\text{F}$, $R_L=150\text{ }\Omega$

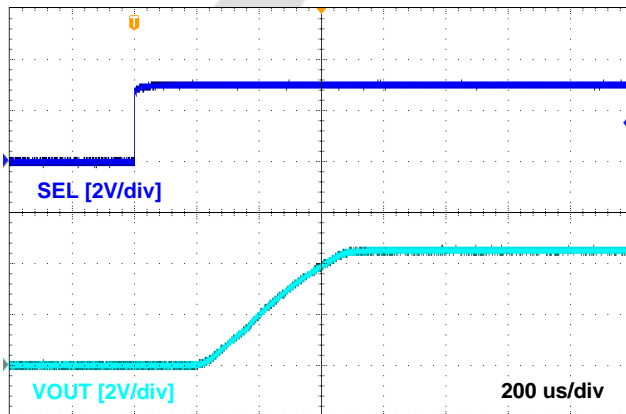


Figure 12. Turn-On Response
 $V_{IN1}=4.5\text{ V}$, $C_{IN}=0.1\text{ }\mu\text{F}$, $C_{OUT}=1.0\text{ }\mu\text{F}$, $R_L=150\text{ }\Omega$

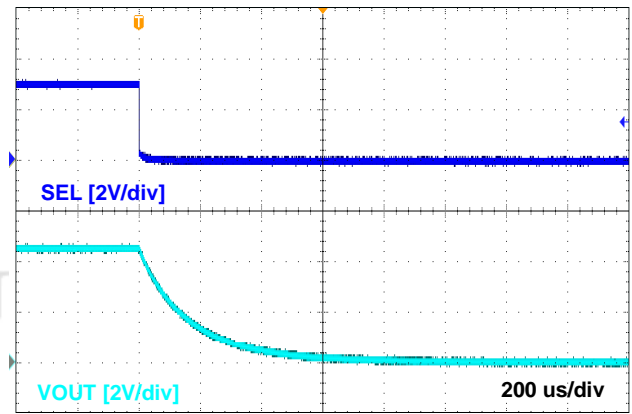


Figure 13. Turn-Off Response
 $V_{IN1}=4.5\text{ V}$, $C_{IN}=0.1\text{ }\mu\text{F}$, $C_{OUT}=1.0\text{ }\mu\text{F}$, $R_L=150\text{ }\Omega$

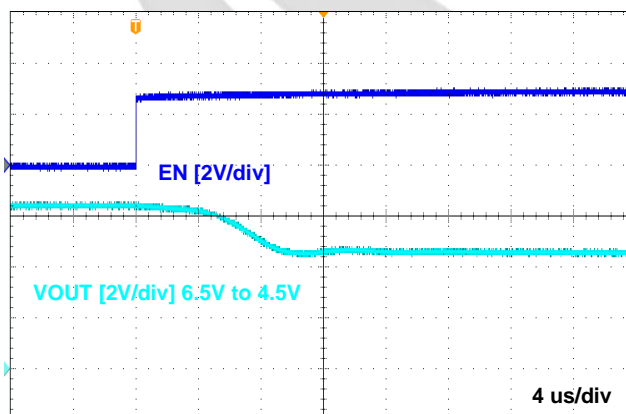


Figure 14. V_{OUT} Switchover from 5 V to 3.3 V
 $V_{IN1}=6.5\text{ V}$, $V_{IN2}=4.5\text{ V}$, $C_{IN}=1.0\text{ }\mu\text{F}$, $C_{OUT}=1.0\text{ }\mu\text{F}$, $R_L=150\text{ }\Omega$

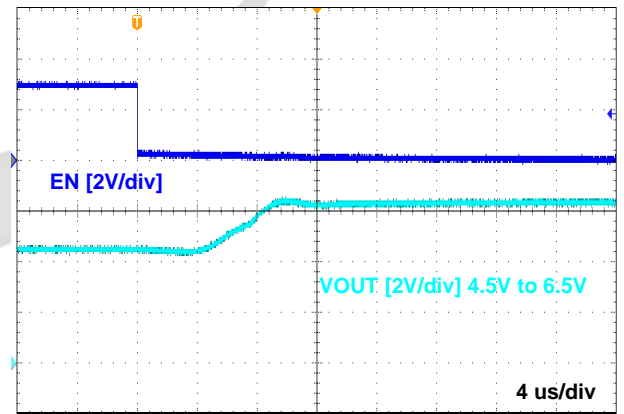


Figure 15. V_{OUT} Switchover from 3.3 V to 5 V
 $V_{IN1}=6.5\text{ V}$, $V_{IN2}=4.5\text{ V}$, $C_{IN}=1.0\text{ }\mu\text{F}$, $C_{OUT}=1.0\text{ }\mu\text{F}$, $R_L=150\text{ }\Omega$

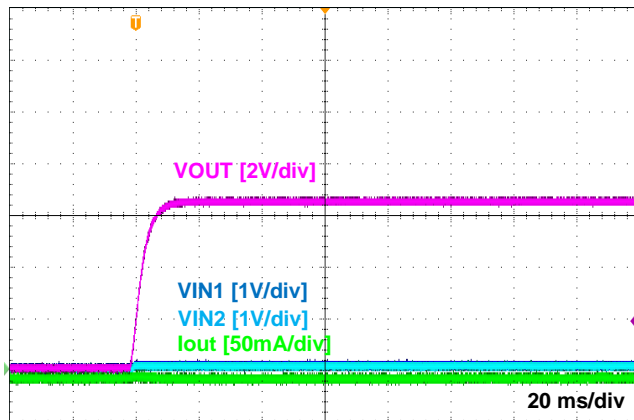


Figure 16. Reverse Current Blocking When Disabled
 $V_{IN1} = V_{IN2} = 0\text{ V}$, $V_{OUT} = 0\text{ V to } 6.5\text{ V}$, $C_{IN} = 1.0\text{ }\mu\text{F}$, $C_{OUT} = 1.0\text{ }\mu\text{F}$,
 $EN = SEL = 0\text{ V}$

APPLICATION INFORMATION

The GLF4020 is a fully integrated 2 A Power Mux with a fixed slew rate control to limit the inrush current during device turn on. The GLF4020 also has a wide voltage operating range from 2.5 V to 6.5 V. In the off state, the GLF4020 consumes very low leakage current to avoid unwanted power drain from limited input power supplies.

Input Source Selection

By changing the state of the SEL and EN pins, the GLF4020 offers the automatic as well as the manual input selection mode. In each mode, the VOUT connects to one input source.

Input Capacitor

A capacitor is recommended to be placed close to the V_{IN} pin to reduce the voltage drop on the input power rail caused by transient inrush current at start-up. A higher input capacitor value can be used to further attenuate the input voltage drop.

Input Voltage Spike Reduction

In steady state condition, the voltages at input pins almost equal to the input power sources. However, at the transient time when the power source is plugged in, a spike voltage will be induced at input pin. The level of the voltage spike is determined by the parasitic inductance between power source and input pin as well as the change rate of input current. The longer length between power source and input pin, the faster change rate of input current, the larger voltage spike. If the spike voltage level exceeds the absolute maximum rated input voltage, it may damage the chip permanently. Below is the waveform when a 6.0 V power source is “hot” plugged in, and the voltage spike can be up to 9.1 V. A “hot” plug-in is not recommended all the time.

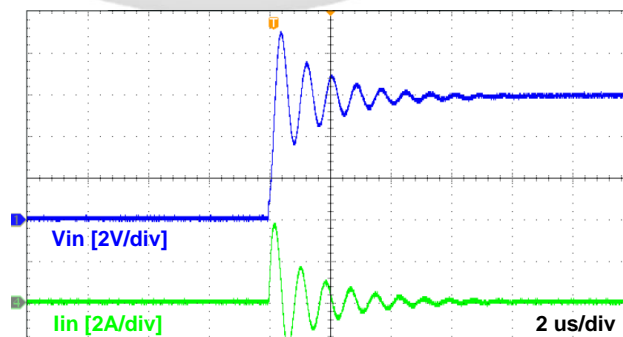


Figure 17. the voltage spike when the power source is “hot” plugged in (IC is disabled)

The voltage spikes are tested with different wire length between the power source and input pin. The results are shown in the table below.

V _{IN} (V)	Wire Length (Cm)	V _{IN_spike} (V)
6.0	1	7.0
	3	7.6
	5	9.1

To avoid unexpected voltage spike, a resistor is recommended in series with input capacitor. The circuit is shown in Figure 18.

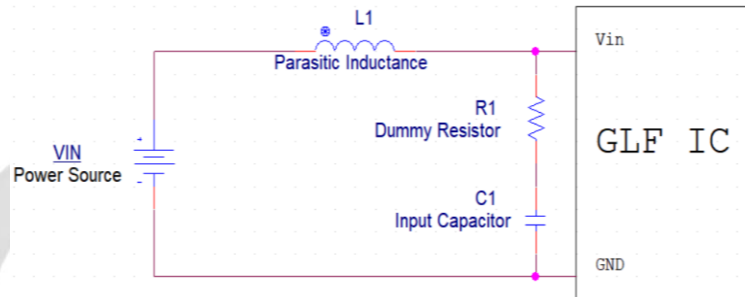


Figure 18. Reduction of voltage spike with a dummy resistor in series with input capacitor

The voltage spike is reduced from 9.1 V (Figure 17) to 6.8 V (Figure 19) by a 1 Ohm dummy resistor which is in series with the input capacitor at same external conditions, which shows a safe voltage spike less than 7 V_{Abs}.

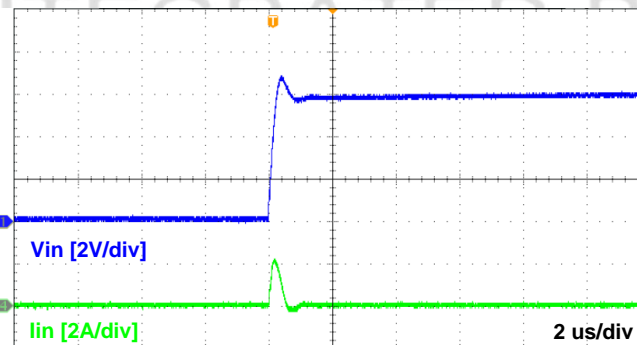


Figure 19. the voltage spike is reduced by the dummy resistor

Several combinations of wire length and dummy resistors are selected for different designs. Test results are shown in the following table. The test results show that the dump resistor can help reduce the voltage spike, and the designers can select proper value resistor in the designs based on the application conditions.

V _{IN} (V)	Dummy Resistor (Ω)	Wire Length (Cm)	V _{IN_spike} (V)
6.0	1.0	1	6.4
		3	6.5
		5	6.8
	2.2	1	6.1
		3	6.3
		5	6.4
	3.6	1	6.0
		3	6.0
		5	6.1

Output Capacitor

An output capacitor is recommended to minimize voltage undershoot on the output pin during the transition when the switch is turned off. Undershoot can be caused by parasitic inductance from board traces or intentional load inductances. If load inductances do exist, use of an output capacitor can improve output voltage stability and system reliability. The C_{OUT} capacitor should be placed close to the VOUT and GND pins.

Reverse Current Blocking

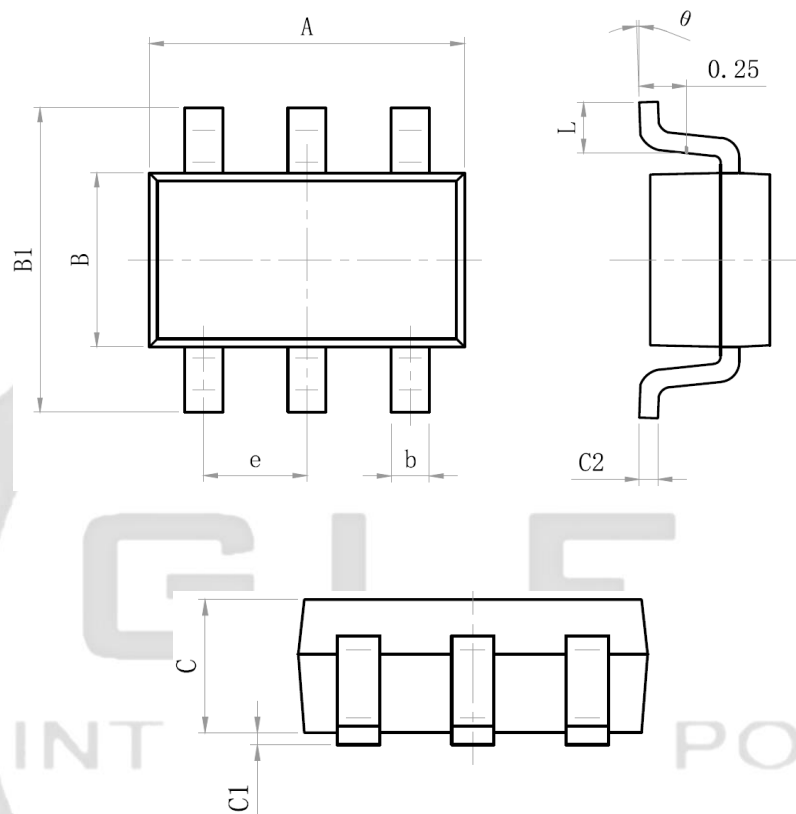
The GLF4020 also prevents the reverse current from the output voltage when both switches are turned off at $EN = SEL = 0\text{ V}$.

Board Layout

All traces should be as short as possible to minimize parasitic inductance effect. Wide traces for VIN, VOUT, and GND will help reduce signal degradation and parasitic effects during dynamic operations as well as improve the thermal performance at high load current.



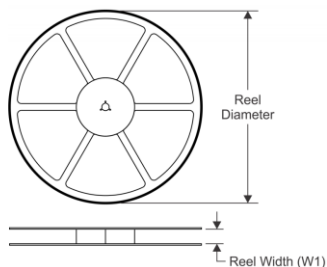
PACKAGE OUTLINE



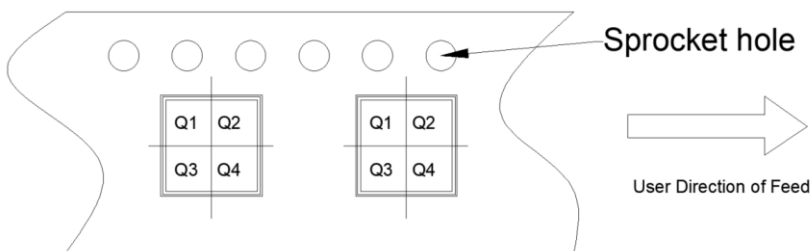
Size Mark	Min (mm)	Max (mm)	Size Mark	Min (mm)	Max (mm)
A	2.82	3.02	C	1.05	1.15
e	0.95 (BSC)		C1	0.03	0.15
b	0.28	0.45	C2	0.12	0.23
B	1.50	1.70	L	0.35	0.55
B1	2.60	3.00	θ	0°	8°

TAPE AND REEL INFORMATION

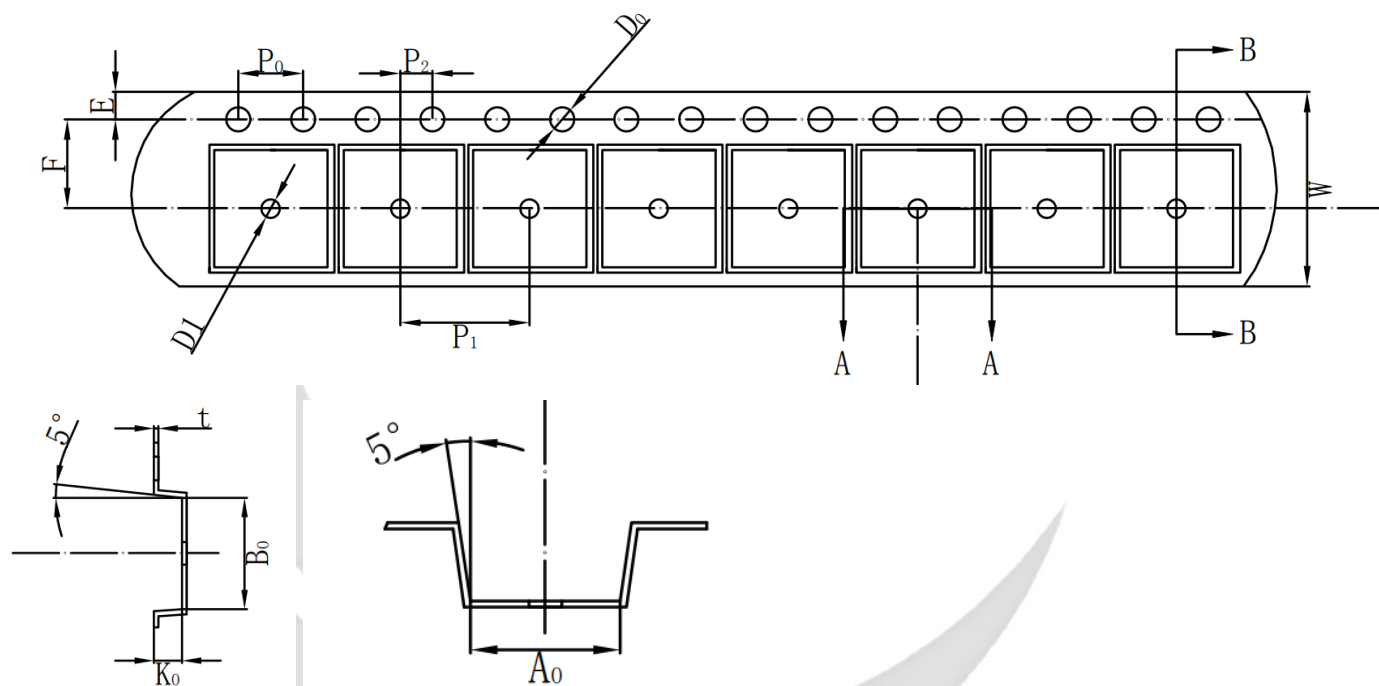
REEL DIMENSIONS



QUADRANT ASSIGNMENTS PIN 1 ORIENTATION TAPE



TAPE DIMENSIONS



Device	Package	Pins	SPQ	Reel Diameter(mm)	Reel Width W1	A0	B0	K0	P1	W	Pin1
GLF4020-T2G7	SOT23-6	6	3000	178	9	3.25	3.30	1.38	4	8	Q3

Remark:

A0: Dimension designed to accommodate the component width

B0: Dimension designed to accommodate the component length

C0: Dimension designed to accommodate the component thickness

W: Overall width of the carrier tape

P1: Pitch between successive cavity centers

SPECIFICATION DEFINITIONS

Document Type	Meaning	Product Status
Target Specification	This is a target specification intended to support exploration and discussion of critical needs for a proposed or target device. Spec limits including typical, minimum, and maximum values are desired, or target, limits. GLF reserves the right to change limits at any time without warning or notification. A target specification in no way guarantees future production of the device in question.	Design / Development
Preliminary Specification	This is a draft version of a product specification. The specification is still under internal review and subject to change. GLF reserves the right to change the specification at any time without warning or notification. A preliminary specification in no way guarantees future production of the device in question.	Qualification
Product Specification	This document represents the anticipated production performance characteristics of the device.	Production

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