GLF72525

Ultra-Low Current Consumption N-channel Power Load Switch with Low Input Voltage Range and Reverse Current Blocking

Product Specification

DESCRIPTION

The GLF72525 Load Switch is a fully integrated 4 A NMOS power load switch with I_QSmart™ advanced technology. The device is targeted for the mobile computing and data storage markets as a high performance solution for load switch applications.

The GLF72525 has a constant low on-resistance of 9.0 mΩ at the full input voltage range. The fixed rise time helps prevent undesirable inrush current when turned on and the internal EN pin pulldown resistor ensures the device remains in the shutdown mode when disabled. In shutdown mode the GLF72525 draws only 14 nA typical at 3.6 V input supply voltage.

The GLF72525 features a reverse current blocking protection, when GLF72525 is disabled. This function can prevents reverse current flowing from the output to the input source.

The GLF72525 is available in a wafer level chip scale package (WLCSP) measuring 0.97 mm x 1.47 mm x 0.55 mm with a 0.5 mm pitch. This allows the user to save board space and increase cost savings.

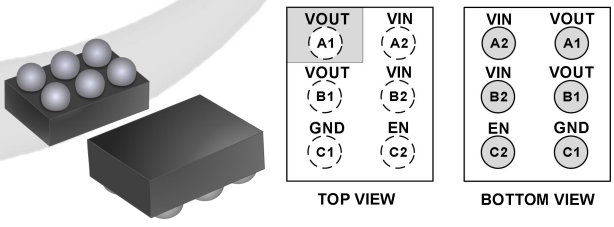
FEATURES

- Supply Voltage Range: 0.7 V to 3.6 V
- Low R_{ON}: 9.0 mΩ Typ
- I_{OUT} Max: 4 A
- Ultra-Low I_Q:
  - 5.6 μA Typ at 0.7 V_{IN}
  - 3.8 μA Typ at 0.8 V_{IN}
  - 8.8 μA Typ at 3.6 V_{IN}
- Ultra-Low I_{SD}: 14 nA Typ @ 3.6 V_{IN}
- Controlled V_{OUT} Turn-on Time
  - 111 μs at 0.7 V_{IN}
  - 113 μs at 0.8 V_{IN}
  - 87 μs at 3.6 V_{IN}
- Internal EN Pull-Down Resistor
- Integrated Output Discharge Switch
- Reverse Current Blocking Protection When Disabled
- Operating Temperature Range: - 40 °C to 105 °C
- HBM: 8 kV, CDM: 2 kV
- 0.97 mm x 1.47 mm x 0.55 mm, 6 Bumps Wafer Level Chip Scale Package

APPLICATIONS

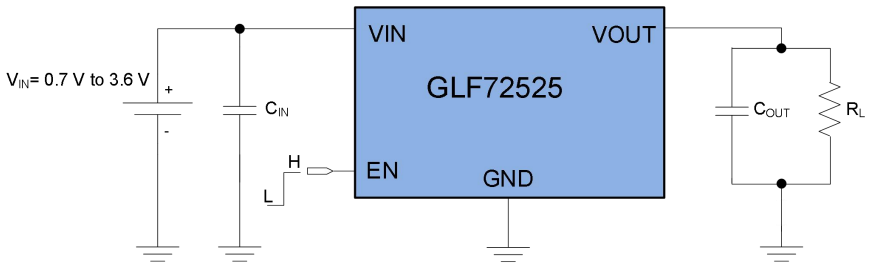
- Data Storage, SSD
- Wearables
- Low Power Subsystems

PACKAGE



0.97 mm x 1.47 mm x 0.55 mm, 0.5 mm Pitch

APPLICATION DIAGRAM



DEVICE ORDERING INFORMATION

Part Number	Top Mark	R_{ON} Typ. at Vin Range	Output Discharge	EN Activity
GLF72525	FJ	9.0 mΩ	85 Ω	High

FUNCTIONAL BLOCK DIAGRAM

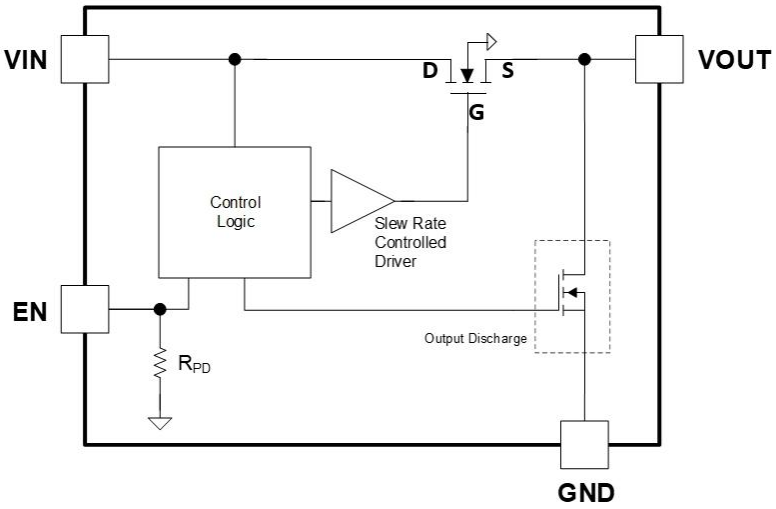


Figure 1. Functional Block Diagram

PIN CONFIGURATION

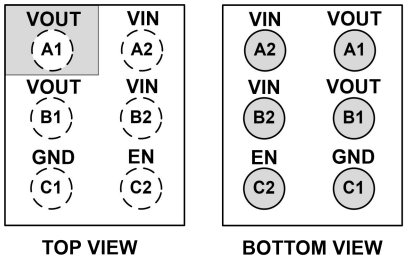


Figure 2. 0.97 mm x 1.47 mm x 0.55 mm WLCSP

PIN DEFINITION

Pin #	Name	Description
A1, B1	V_{OUT}	Switch Output
A2, B2	V_{IN}	Switch Input. Supply Voltage for IC
C1	GND	Ground
C2	EN	Enable to control the switch

ABSOLUTE MAXIMUM RATINGS

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
VIN, VOUT, EN	Each Pin Voltage Range to GND		-0.3	4	V
I_{OUT}	Maximum Continuous Switch Current			4	A
P_D	Power Dissipation at T_A = 25°C			1.2	W
T_{STG}	Storage Junction Temperature		-65	150	°C
θ_{JA}	Thermal Resistance, Junction to Ambient			85	°C/W
ESD	Electrostatic Discharge Capability	Human Body Model, JESD22-A114	8		kV
		Charged Device Model, JESD22-C101	2		

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Max.	Unit
VIN	Supply Voltage	0.7	3.6	V
T_A	Ambient Operating Temperature	-40	+105	°C

ELECTRICAL CHARACTERISTICS

V_{IN} = 0.7 V to 3.6 V and T_A = 25 °C unless otherwise noted.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Units
Basic Operation							
I_Q	Quiescent Current	EN = Enable, I_{OUT} = 0 mA, V_{IN} = 0.7 V			5.6		μA
		EN = Enable, I_{OUT} = 0 mA, V_{IN} = 0.8 V			3.8		
		EN = Enable, I_{OUT} = 0 mA, V_{IN} = 1.5 V			3.1		
		EN = Enable, I_{OUT} = 0 mA, V_{IN} = 2.5 V			5.1		
		EN = Enable, I_{OUT} = 0 mA, V_{IN} = 3.0 V			6.5		
		EN = Enable, I_{OUT} = 0 mA, V_{IN} = 3.6 V			8.8		
		EN = Enable, I_{OUT} = 0 mA, V_{IN} = 3.6 V, Ta = 85 °C			16		
		EN = Enable, I_{OUT} = 0 mA, V_{IN} = 3.6 V, T_A = 105 °C			39		
I_{SD}	Shutdown Current	EN = Disable, I_{OUT} = 0 mA, V_{IN} = 0.7 V			6	20	nA
		EN = Disable, I_{OUT} = 0 mA, V_{IN} = 0.8 V			6		
		EN = Disable, I_{OUT} = 0 mA, V_{IN} = 1.5 V			7		
		EN = Disable, I_{OUT} = 0 mA, V_{IN} = 2.5 V			8		
		EN = Disable, I_{OUT} = 0 mA, V_{IN} = 3.0 V			9		
		EN = Disable, I_{OUT} = 0 mA, V_{IN} = 3.6 V			14	35	
		EN = Disable, I_{OUT} = 0 mA, V_{IN} = 3.6 V, Ta = 85 °C			550		
		EN = Disable, I_{OUT} = 0 mA, V_{IN} = 3.6 V, T_A = 105 °C			2.1		μA
R_{ON}	On-Resistance	V_{IN}= 0.7 V to 3.6 V, I_{OUT}= 300 mA	T_A= 25 °C		9	12	mΩ
			T_A= 85 °C		10		
			T_A= 105 °C		11		
R_{DSC}	Output Discharge Resistance	EN= Low , I_{FORCE}= 10 mA			85		Ω
V_{IH}	EN Input Logic High Voltage	V_{IN} = 0.7 V to 1.5 V		0.7			V
		V_{IN} = 1.5 V to 3.6 V		1.1			V
V_{IL}	EN Input Logic Low Voltage	V_{IN} = 0.7 V to 1.5 V				0.15	V
		V_{IN} = 1.5 V to 3.6 V				0.4	V
R_{EN}	EN pull down resistance	V_{EN} = 3.3 V			10		MΩ
Switching Characteristics (1)							
t_{dON}	Turn-On Delay Time R_{OUT} = 150 Ω, C_{OUT} = 5.0 μF	V_{IN}= 0.7 V			40		μs
		V_{IN}= 0.8 V			52		
		V_{IN}= 1.2 V			48		
		V_{IN}= 2.5V			14		
		V_{IN}= 3.6 V			5		
t_R	V_{OUT} Rise Time R_{OUT} = 150 Ω, C_{OUT} = 5.0 μF	V_{IN}= 0.7 V			71		
		V_{IN}= 0.8 V			61		
		V_{IN}= 1.2 V			65		
		V_{IN}= 2.5V			77		
		V_{IN}= 3.6 V			82		
t_{dOFF}	Turn-Off Delay Time R_{OUT} = 150 Ω, C_{OUT} = 5.0 μF	V_{IN}= 0.7 V			8		
		V_{IN}= 0.8 V			4		
		V_{IN}= 1.2 V			3		
		V_{IN}= 2.5V			3		

ELECTRICAL CHARACTERISTICS (continued)

V_{IN} = 0.8 V to 3.6 V and T_A = 25 °C unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Switching Characteristics (1) **(continued)**						
t_F	V_{OUT} Fall Time R_{OUT} = 150 Ω, C_{OUT} = 5.0 µF	V_{IN}= 0.7 V		86		µs
		V_{IN}= 0.8 V		82		
		V_{IN}= 1.2 V		91		
		V_{IN}= 2.5V		99		
		V_{IN}= 3.6 V		105		

Notes: 1. By design; characterized, not production tested. $t_{ON} = t_{dON} + t_R$, $t_{OFF} = t_{dOFF} + t_F$

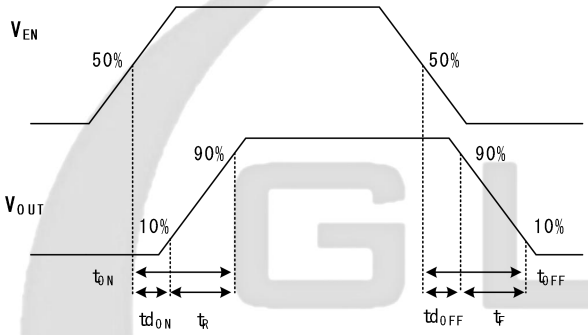


Figure 3. Timing Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

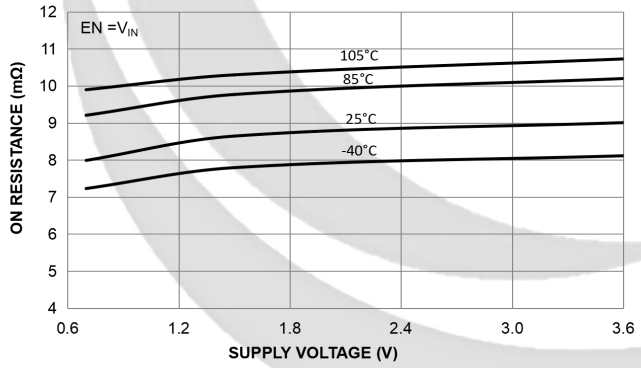


Figure 4. On-Resistance vs. Supply Voltage

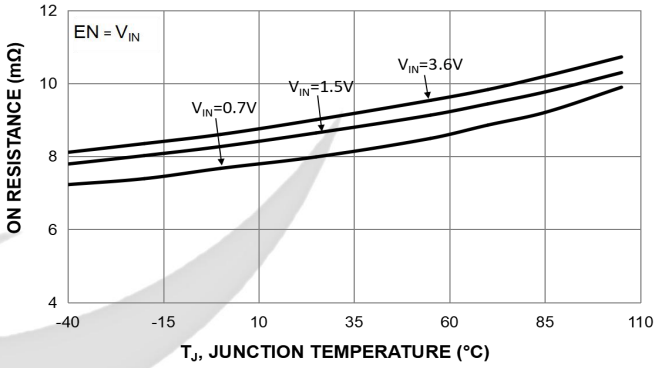


Figure 5. On-Resistance vs. Temperature

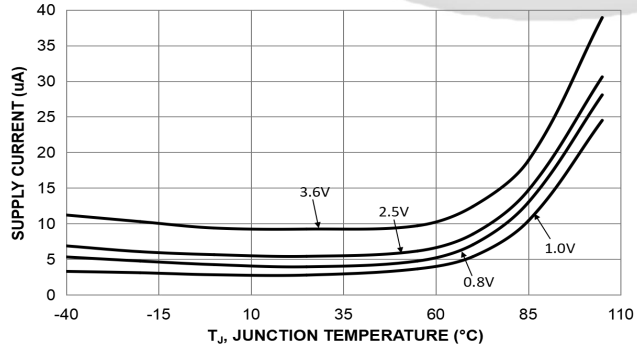


Figure 6. Quiescent Current vs. Temperature

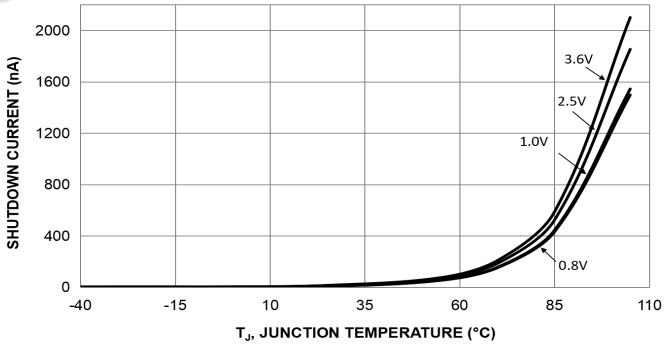


Figure 7. Shutdown Current vs Temperature

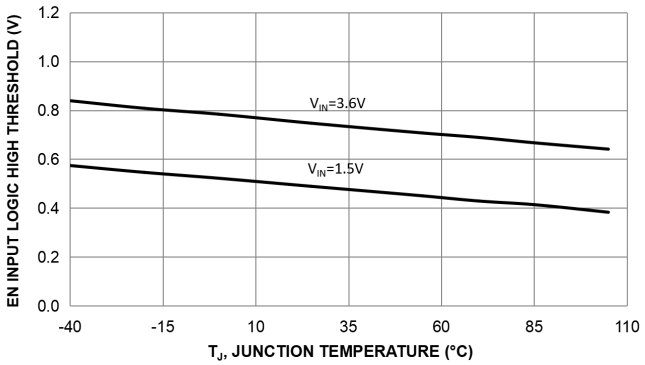


Figure 8. EN Input Logic High Threshold Vs. Temperature

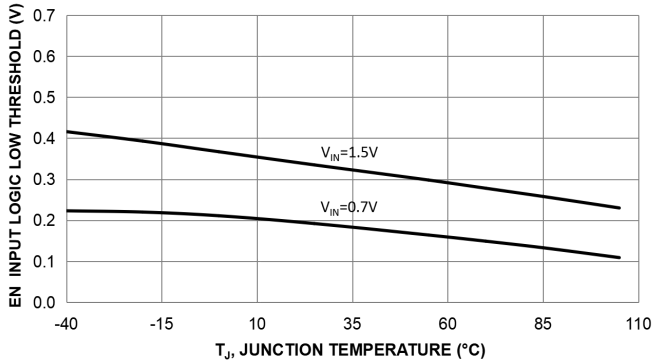


Figure 9. EN Input Logic Low Threshold Vs. Temperature

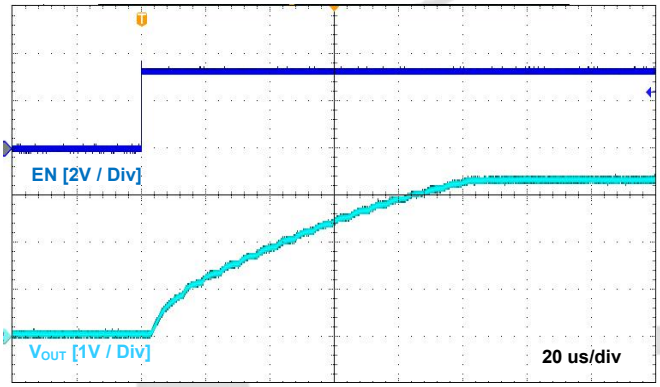


Figure 10. Turn-On Response

V_{IN}= 3.3 V, C_{IN}= 1.0 µF, C_{OUT}= 5.0 µF, R_L=150 Ω

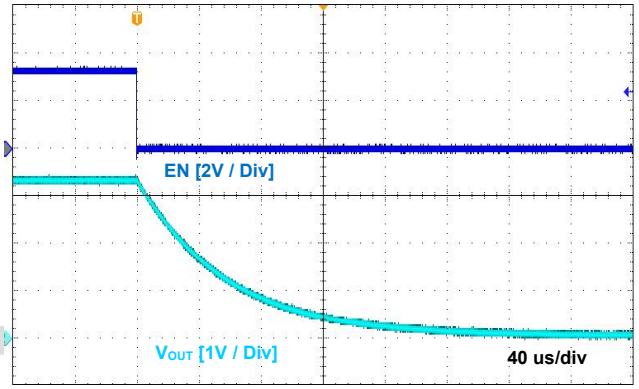


Figure 11. Turn-Off Response

V_{IN}= 3.3 V, C_{IN}= 1.0 µF, C_{OUT}= 5.0 µF, R_L=150 Ω

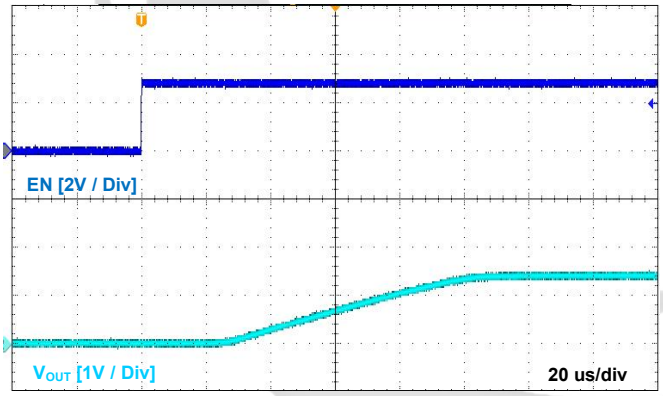


Figure 12. Turn-On Response

V_{IN}= 0.7 V, C_{IN}= 1.0 µF, C_{OUT}= 5.0 µF, R_L=150 Ω

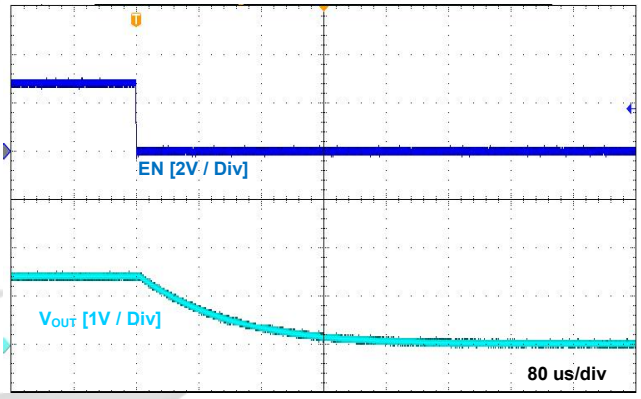


Figure 13. Turn-Off Response

V_{IN}= 0.7 V, C_{IN}= 1.0 µF, C_{OUT}= 5.0 µF, R_L=150 Ω

APPLICATION INFORMATION

The GLF72525 is a fully integrated 4 A NMOS power load switch with fixed slew rate control to limit the inrush current during turn on. Each device is capable of operating over a wide input range with very low on-resistance to reduce conduction loss. In the off state, these devices consume very low leakage current, avoiding unwanted standby current from the input power supply. The GLF72525 is available in the 0.97 mm x 1.47 mm wafer level chip scale package with 6 bumps at 0.5 mm pitch to save space in compact applications.

Input Capacitor

A capacitor is recommended to be placed close to the V_{IN} pin to reduce the voltage drop on the input power rail caused by transient inrush current at start-up. A higher input capacitor value can be used to further attenuate the input voltage drop.

Output Capacitor

An output capacitor is recommended to minimize voltage undershoot on the output pin during the transition when the switch is turned off. Undershoot can be caused by parasitic inductance from board traces or intentional load inductances. If load inductances do exist, use of an output capacitor can improve output voltage stability and system reliability. The C_{OUT} capacitor should be placed close to the VOUT and GND pins.

Reverse Current Blocking

The GLF72525 has a built-in reverse current blocking protection, when the device is disabled. The reverse current blocking protection is activated to prevent the reverse current from the VOUT to the VIN source.

EN pin

The GLF72525 can be activated by EN pin high. Note that the EN pin has an internal pull-down resistor to maintain a reliable status without EN signal applied from an external controller.

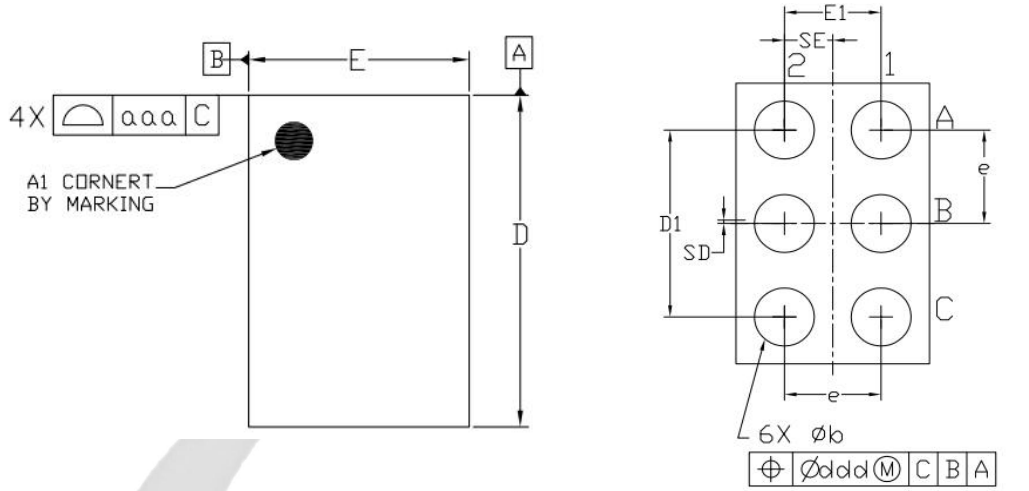
Output Discharge Function

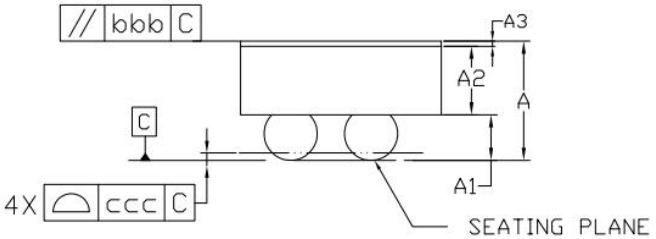
The GLF72525 has an internal discharge N-channel FET switch on the VOUT node. When EN signal turns the main power FET to an off state, the N-channel switch turns on to discharge an output capacitor quickly.

Board Layout

All traces should be as short as possible to minimize parasitic inductance effect. Wide traces for VIN, VOUT, and GND will help reduce signal degradation and parasitic effects during dynamic operations as well as improve the thermal performance at high load current.

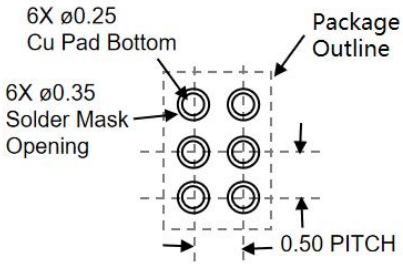
PACKAGE OUTLINE





Dimensional Ref.			
REF.	Min.	Nom.	Max.
A	0.500	0.550	0.600
A1	0.225	0.250	0.275
A2	0.250	0.275	0.300
A3	0.020	0.025	0.030
D	1.460	1.470	1.485
E	0.960	0.970	0.985
D1	0.950	1.000	1.050
E1	0.450	0.500	0.550
b	0.260	0.310	0.360
e	0.500 BSC		
SD	0.000 BSC		
SE	0.250 BSC		
Tol. of Form&Position			
aaa	0.10		
bbb	0.10		
ccc	0.05		
ddd	0.05		

Recommended Footprint

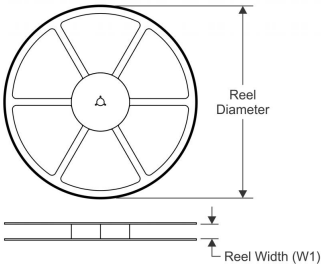


Notes

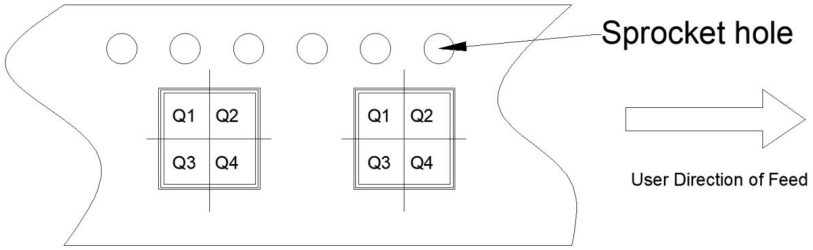
1. ALL DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGRESS)
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.
3. A3: BACKSIDE LAMINATION

TAPE AND REEL INFORMATION

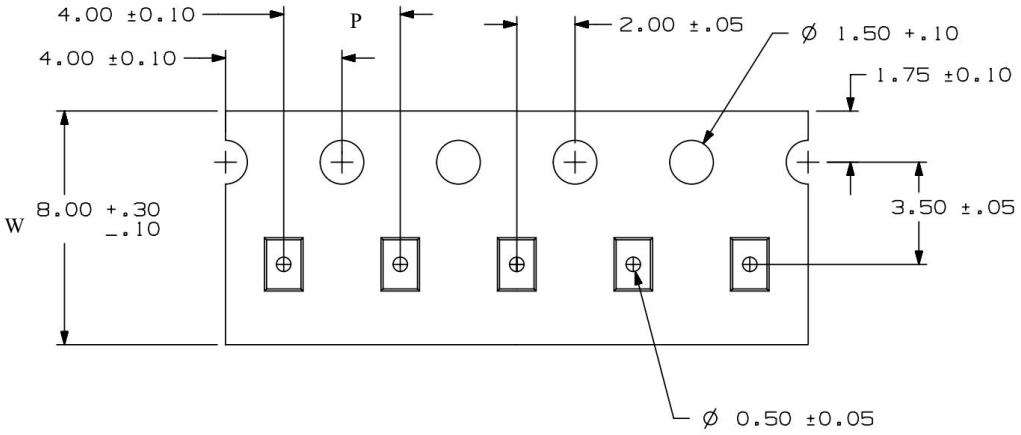
REEL DIMENSIONS

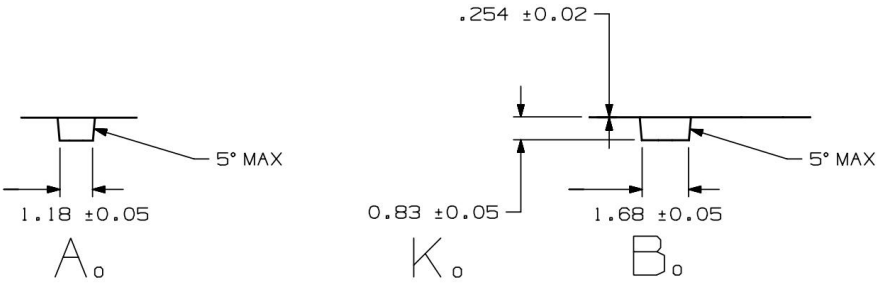


QUADRANT ASSIGNMENTS PIN 1 ORIENTATION TAPE



TAPE DIMENSIONS





Device	Package	Pins	SPQ	Reel Diameter (mm)	Reel Width W1	A0	B0	K0	P	W	Pin1
GLF72525	WLCSP	6	3000	180	9	1.18	1.68	0.83	4	8	Q1

Remark:

A0: Dimension designed to accommodate the component width

B0: Dimension designed to accommodate the component length

C0: Dimension designed to accommodate the component thickness

W: Overall width of the carrier tape

P: Pitch between successive cavity centers

SPECIFICATION DEFINITIONS

Document Type	Meaning	Product Status
Target Specification	This is a target specification intended to support exploration and discussion of critical needs for a proposed or target device. Spec limits including typical, minimum, and maximum values are desired, or target, limits. GLF reserves the right to change limits at any time without warning or notification. A target specification in no way guarantees future production of the device in question.	Design / Development
Preliminary Specification	This is a draft version of a product specification. The specification is still under internal review and subject to change. GLF reserves the right to change the specification at any time without warning or notification. A preliminary specification in no way guarantees future production of the device in question.	Qualification
Product Specification	This document represents the anticipated production performance characteristics of the device.	Production

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