

DESCRIPTION

The GLF71311T is an **ultra-thin**, ultra-efficiency, 2A rated, Load Switch with integrated slew rate control. The best in class efficiency makes it an ideal chose for use in IoT, mobile, and wearable electronics.

The GLF71311T features ultra-efficient I_QSmart™ technology that supports the lowest quiescent current (I_Q) and shutdown current (I_{SD}) in the industry. Low I_Q and I_{SD} solutions help designers to reduce parasitic leakage current, improve system efficiency, and increase battery lifetime.

The GLF71311T integrated slew rate control can also enhance system reliability by mitigating bus voltage swings during switching events. Where uncontrolled switches can generate high inrush currents that result in voltage droop and/or bus reset events, the GLF slew rate control specifically limits inrush currents during turn-on to minimize voltage droop.

GLF71311T Load Switch devices support an industry leading wide input voltage range and helps to improve operating life and system robustness. Furthermore, one device can be used in multiple voltage rail applications which helps to simplify inventory management and reduce operating cost.

GLF71311T Load Switch device is small utilizing a wafer level chip scale package with 4 bumps in a 0.97 mm x 0.97 mm die size and a 0.5 mm bump pitch. GLF71311T is ultra-thin: 0.35 mm Typ, 0.4 mm Max.

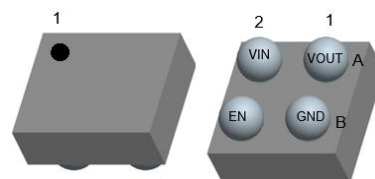
FEATURES

- Ultra-Low I_Q: 7 nA Typ @ 5.5 V_{IN}
- Ultra-Low I_{SD}: 28 nA Typ @ 5.5 V_{IN}
- Low R_{ON}: 31 mΩ Typ @ 5.5 V_{IN}
- I_{OUT} Max: 2 A
- Wide Input Range: 1.1 V to 5.5 V
6 Vabs max
- Controlled Rise Time: 335 us at 3.3 V_{IN}
- Internal EN Pull-Down Resistor
- Integrated Output Discharge Switch
- Ultra-Small: 0.97 mm x 0.97 mm
- Ultra-Thin: 0.35 mm Typ., 0.4 mm Max.

APPLICATIONS

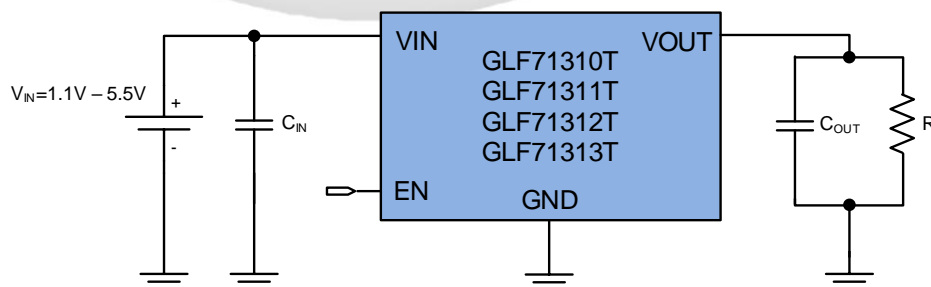
- Powered Credit Cards
- Thin Mobile Devices & Wearables
- Low Power Subsystems

PACKAGE



0.97 mm x 0.97 mm x 0.35 mm WLCSP

APPLICATION DIAGRAM



ALTERNATE DEVICE OPTIONS

Part Number	Top Mark	R _{ON} (Typ) at 5.5V	Output Discharge	EN Activity	Availability
GLF71310T	BA	31 mΩ	No	High	On Request
GLF71311T	BC	31 mΩ	85Ω	High	Released
GLF71312T	BD	31 mΩ	No	Low	On Request
GLF71313T	BE	31 mΩ	85 Ω	Low	On Request

Contact GLF for more information on alternate device delivery and availability.

FUNCTIONAL BLOCK DIAGRAM

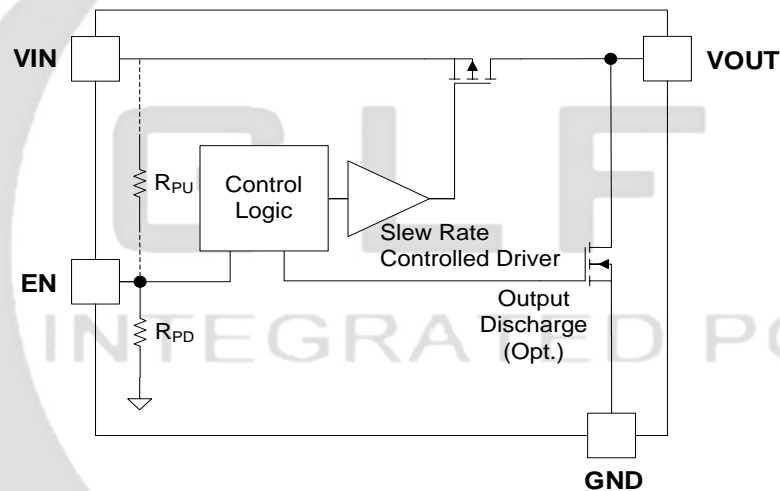
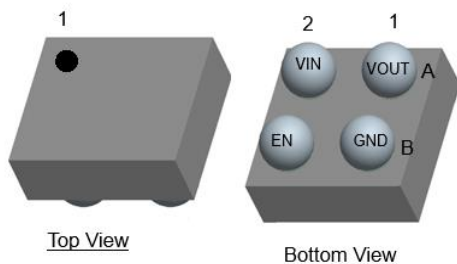


Figure 1. Functional Block Diagram

PIN CONFIGURATION

PIN DEFINITION



Pin #	Name	Description
A1	V _{OUT}	Switch Output
A2	V _{IN}	Switch Input. Supply Voltage for IC
B1	GND	Ground
B2	EN	Enable to control the switch

Figure 2. 0.97 mm x 0.97 mm x 0.35 mm WLCSP

ABSOLUTE MAXIMUM RATINGS

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions; extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V _{IN} , V _{OUT} , V _{EN}	Each Pin Voltage Range to GND		-0.3	6	V
I _{OUT}	Maximum Continuous Switch Current			2	A
P _D	Power Dissipation at T _A = 25 °C			1.2	W
T _{STG}	Storage Junction Temperature		-65	150	°C
T _A	Operating Temperature Range		-40	85	°C
θ _{JA}	Thermal Resistance, Junction to Ambient			85	°C/W
ESD	Electrostatic Discharge Capability	Human Body Model, JESD22-A114	6		kV
		Charged Device Model, JESD22-C101	2		

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Max.	Unit
V _{IN}	Supply Voltage	1.1	5.5	V
T _A	Ambient Operating Temperature	-40	+85	°C

ELECTRICAL CHARACTERISTICS

Values are at $V_{IN} = 3.3\text{ V}$ and $T_A = 25\text{ °C}$ unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Basic Operation						
V_{IN}	Supply Voltage		1.1		5.5	V
I_Q	Quiescent Current ⁽¹⁾	EN = Enable, $I_{OUT}=0\text{ mA}$, $V_{IN} = V_{EN}=5.5\text{ V}$		7	70	nA
		EN= Enable, $I_{OUT}=0\text{ mA}$, $V_{IN}=V_{EN}=5.5\text{ V}$, $T_A=85\text{ °C}$ ⁽⁵⁾		12		
I_{SD}	Shut Down Current	EN = Disable, $I_{OUT}=0\text{ mA}$, $V_{IN}=1.1\text{ V}$		5		nA
		EN = Disable, $I_{OUT}=0\text{ mA}$, $V_{IN}=1.8\text{ V}$		6		
		EN = Disable, $I_{OUT}=0\text{ mA}$, $V_{IN}=3.3\text{ V}$		9	35	
		EN = Disable, $I_{OUT}=0\text{ mA}$, $V_{IN}=4.5\text{ V}$		13		
		EN = Disable, $I_{OUT}=0\text{ mA}$, $V_{IN}=5.5\text{ V}$		28	100	
		EN = Disable, $I_{OUT}=0\text{ mA}$, $V_{IN}=5.5\text{ V}$, $T_A=55\text{ °C}$ ⁽⁵⁾		0.2		uA
		EN = Disable, $I_{OUT}=0\text{ mA}$, $V_{IN}=5.5\text{ V}$, $T_A=85\text{ °C}$ ⁽⁵⁾		1		
R_{ON}	On-Resistance	$V_{IN}=5.5\text{ V}$, $I_{OUT}= 500\text{ mA}$	$T_A=25\text{ °C}$	31	34	mΩ
			$T_A=85\text{ °C}$ ⁽⁵⁾	36		
		$V_{IN}=3.3\text{ V}$, $I_{OUT}= 500\text{ mA}$	$T_A=25\text{ °C}$	36	41	
			$T_A=85\text{ °C}$ ⁽⁵⁾	43		
		$V_{IN}=1.8\text{ V}$, $I_{OUT}= 300\text{ mA}$	$T_A=25\text{ °C}$	52		
		$V_{IN}=1.1\text{ V}$, $I_{OUT}= 100\text{ mA}$	$T_A=25\text{ °C}$	95		
R_{DSC}	Output Discharge Resistance	EN=Low, $I_{FORCE}= 10\text{ mA}$	70	85	100	Ω
V_{IH}	EN Input Logic High Voltage	$V_{IN}=1.1\text{ V} - 1.8\text{ V}$	0.9			V
		$V_{IN}=1.8\text{ V} - 5.5\text{ V}$	1.2			V
V_{IL}	EN Input Logic Low Voltage	$V_{IN}=1.1\text{ V} - 1.8\text{ V}$			0.3	V
		$V_{IN}=1.8\text{ V} - 5.5\text{ V}$			0.4	V
R_{EN}	EN pull down resistance	Internal Resistance		9.5		MΩ
I_{EN}	EN Current	EN=5.5 V			1.0	μA
Switching Characteristics						
t_{dON}	Turn-On Delay ⁽²⁾	$R_L=150\text{ Ω}$, $C_{OUT}=0.1\text{ μF}$		210		μs
t_R	V_{OUT} Rise Time ⁽²⁾			335		
t_{dON}	Turn-On Delay ^(2,5)	$R_L=500\text{ Ω}$, $C_{OUT}=0.1\text{ μF}$		220		
t_R	V_{OUT} Rise Time ^(2,5)			330		
t_{dOFF}	Turn-Off Delay ^(3,4,5)	$R_L=10\text{ Ω}$, $C_{OUT}=0.1\text{ μF}$		0.38		
t_F	V_{OUT} Fall Time ^(3,4,5)			1.3		
t_{dOFF}	Turn-Off Delay ^(3,4,5)	$R_L=500\text{ Ω}$, $C_{OUT}=0.1\text{ μF}$		0.9		
t_F	V_{OUT} Fall Time ^(3,4,5)			16		

- Notes:
- I_Q does NOT include Enable pull down current through the pull down resistor R_{PD} .
 - $t_{ON} = t_{dON} + t_R$
 - $t_{OFF} = t_{dOFF} + t_F$
 - Output discharge path is enabled during off.
 - By design; characterized, not production tested.

TIMING DIAGRAM

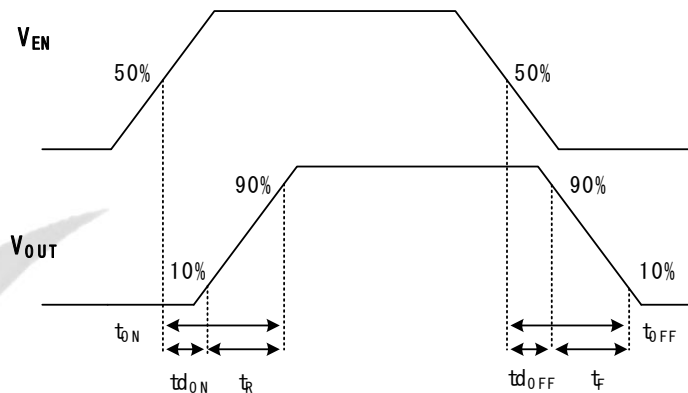


Figure 2. Timing Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

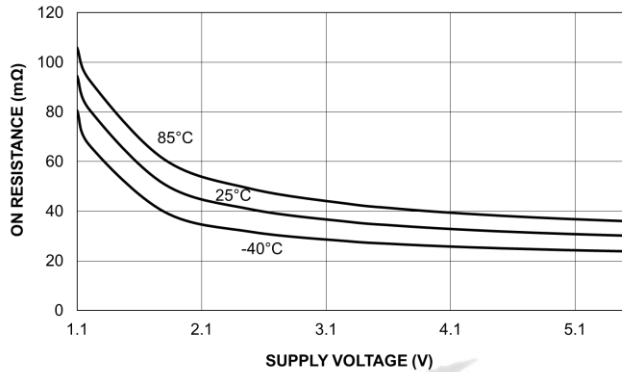


Figure 4. On-Resistance vs. Input Voltage

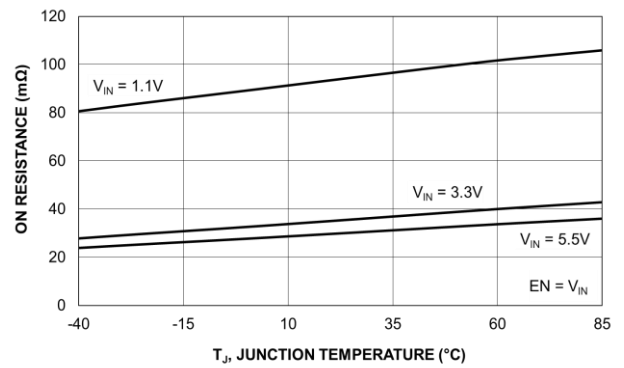


Figure 5. On-Resistance vs. Temperature

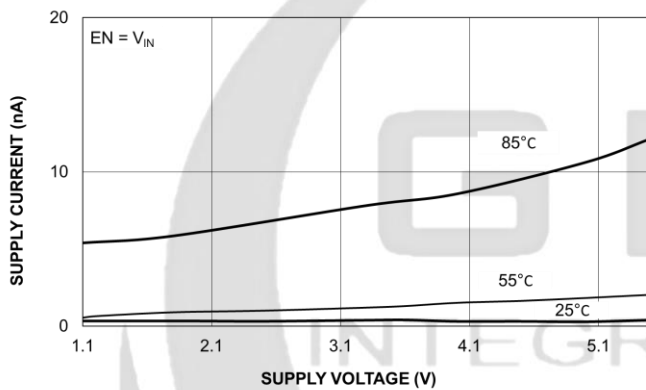


Figure 6. Quiescent Current vs. Input Voltage

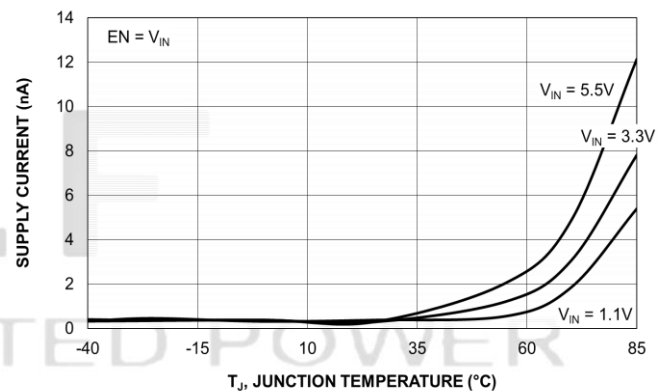


Figure 7. Quiescent Current vs. Temperature

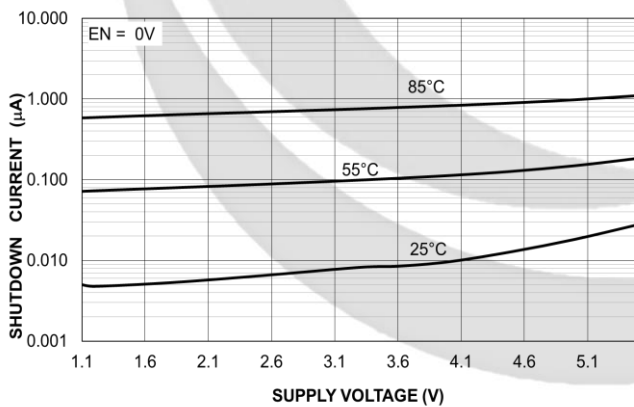


Figure 3. Shut Down Current vs. Input Voltage

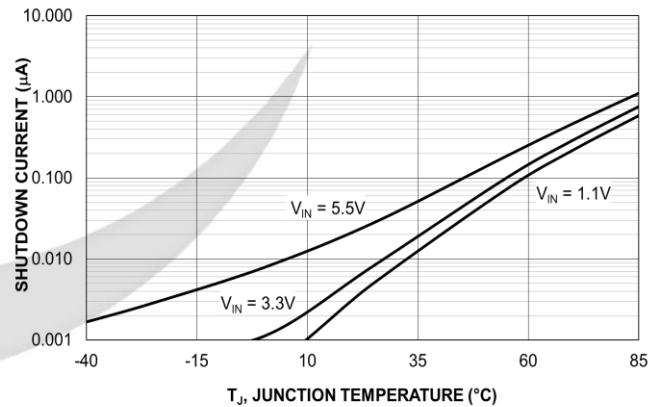


Figure 4. Shut Down Current vs. Temperature

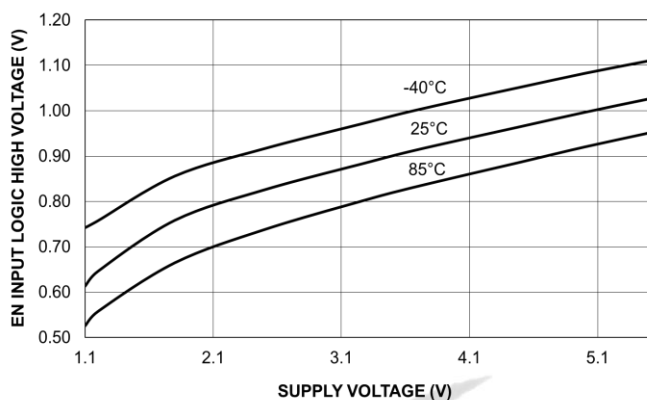


Figure 5. EN Input Logic High Threshold

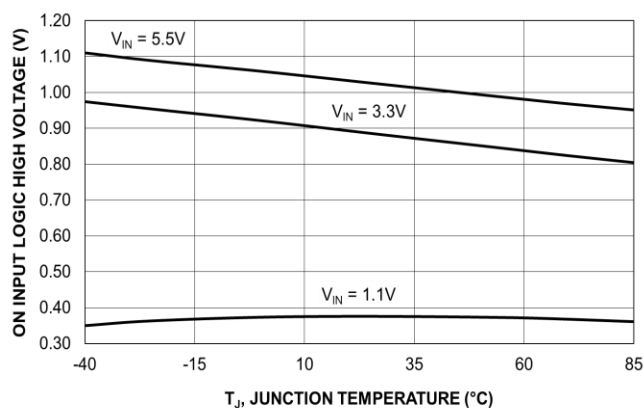


Figure 6. EN Input Logic High Threshold Vs. Temperature

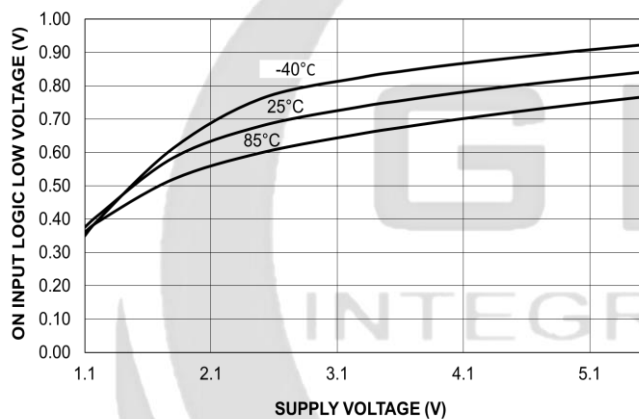


Figure 7. EN Input Logic Low Threshold

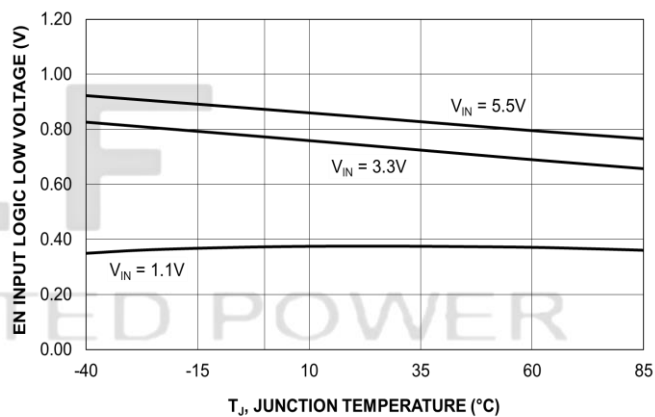


Figure 8. EN Input Logic Low Threshold Vs. Temperature

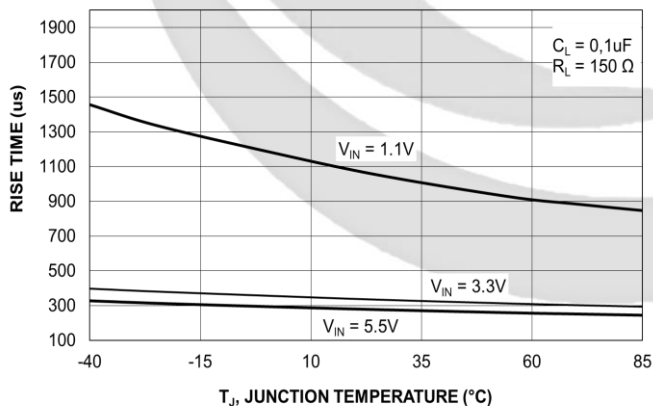


Figure 9. VOUT Rise Time vs. Temperature

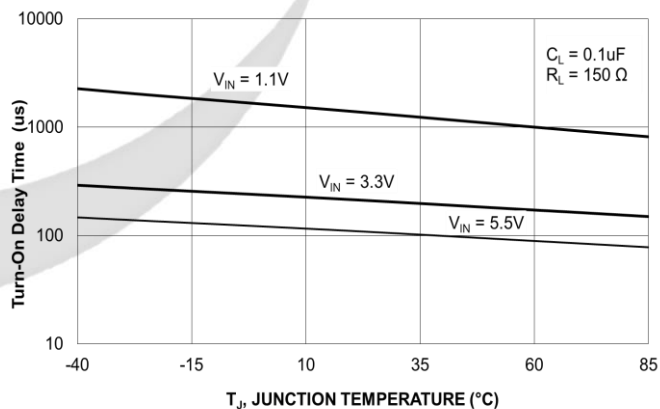


Figure 10. Turn-On Delay Time vs. Temperature

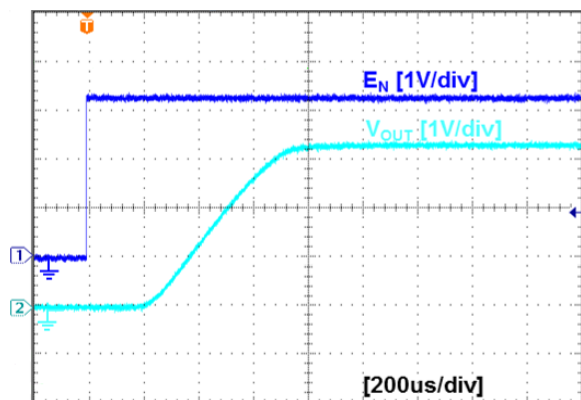


Figure 11. Turn-On Response
 $V_{IN}=3.3\text{ V}$, $C_{IN}=1.0\text{ }\mu\text{F}$, $C_{OUT}=0.1\text{ }\mu\text{F}$, $R_L=10\text{ }\Omega$

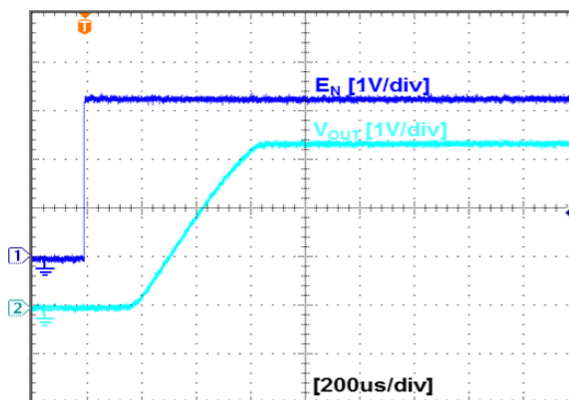


Figure 12. Turn-On Response
 $V_{IN}=3.3\text{ V}$, $C_{IN}=1.0\text{ }\mu\text{F}$, $C_{OUT}=0.1\text{ }\mu\text{F}$, $R_L=500\text{ }\Omega$

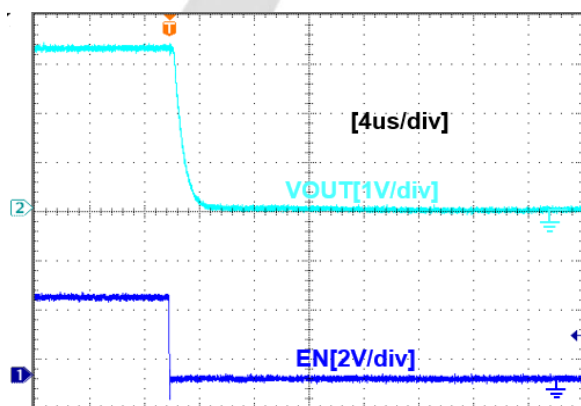


Figure 13. Turn-Off Response, Output Discharge
 $V_{IN}=3.3\text{ V}$, $C_{IN}=1.0\text{ }\mu\text{F}$, $C_{OUT}=0.1\text{ }\mu\text{F}$, $R_L=10\text{ }\Omega$

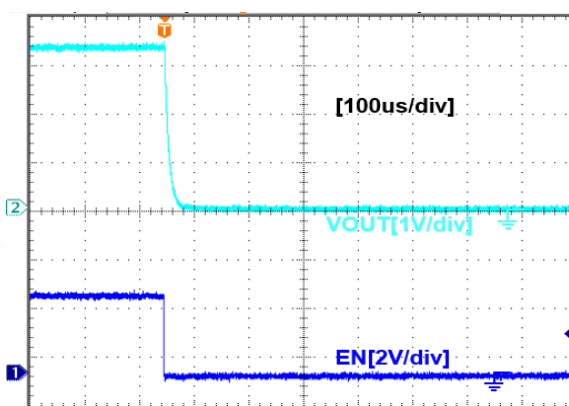


Figure 14. Turn-Off Response, Output Discharge
 $V_{IN}=3.3\text{ V}$, $C_{IN}=1.0\text{ }\mu\text{F}$, $C_{OUT}=0.1\text{ }\mu\text{F}$, $R_L=500\text{ }\Omega$

APPLICATION INFORMATION

The GLF7131xT family of devices are integrated 2 A, Ultra-Efficient IqSmart™ Load Switch devices with a fixed slew rate control to limit the inrush current during turn on. Each device is capable of operating over a wide input range from 1.1 V to 5.5V with very low on-resistance to reduce conduction loss. In the off state, these devices consume very low leakage current to avoid unwanted standby current and save limited input power. The package is a 0.97 mm x 0.97 mm x 0.35 mm wafer level chip scale package, saving space in compact applications. It is constructed using 4 bumps, with a 0.5 mm pitch for manufacturability.

Input Capacitor

The GLF7131xT family of devices do not require an input capacitor. However, to reduce the voltage drop on the input power rail caused by transient inrush current at start-up, a 0.1 μ F capacitor is recommended to be placed close to the V_{IN} pin. A higher input capacitor value can be used to further attenuate the input voltage drop.

Output Capacitor

The GLF7131xT family of devices do not require an output capacitor. However, use of an output capacitor is recommended to mitigate voltage undershoot on the output pin when the switch is turning off. Undershoot can be caused by parasitic inductance from board traces or intentional load inductances. If load inductances do exist, use of an output capacitor can improve output voltage stability and system reliability. The C_{OUT} capacitor should be spaced close to the V_{OUT} and GND pins.

EN pin

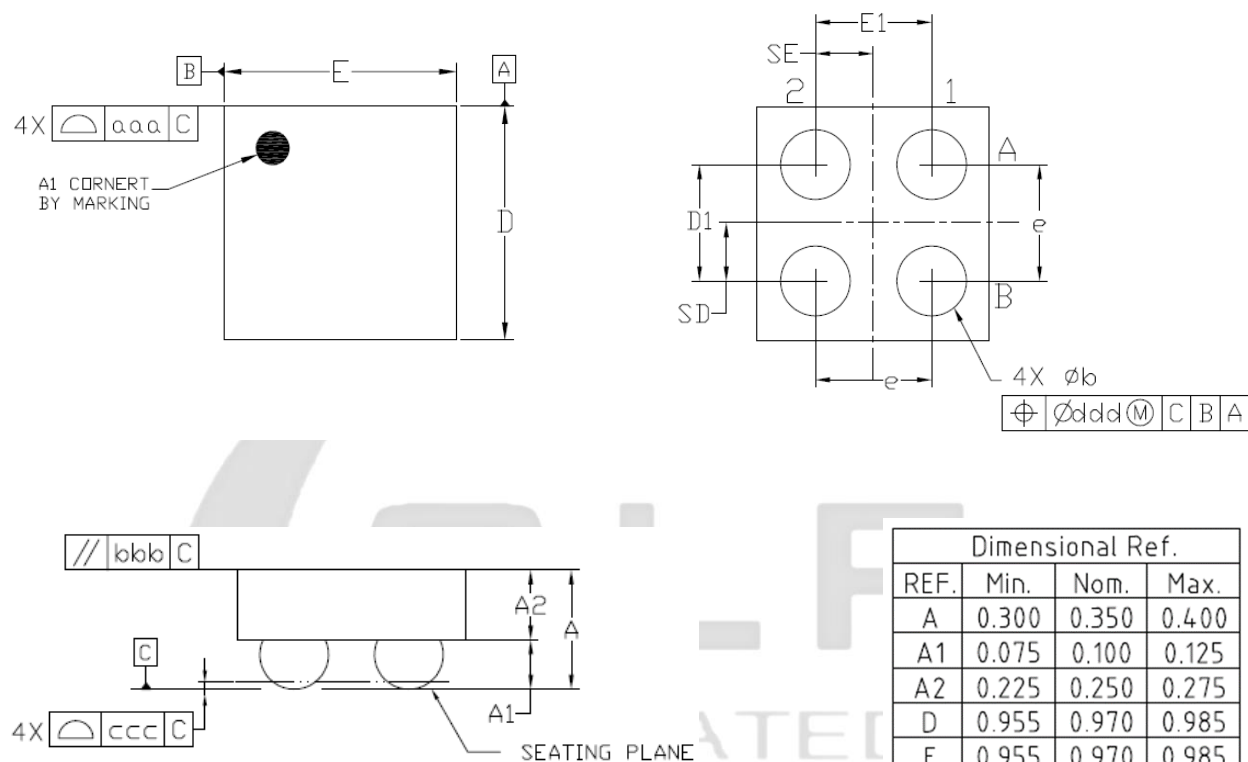
The GLF71310T and GLF71311T can be activated by forcing EN pin high level and GLF71312T and GLF71313T by EN pin low level. Note that the EN pin has an internal pull-down or pull-up resistor to help pull the main switch to a known “off state” when no EN signal is applied from an external controller.

Output Discharge Function

The GLF71311T and GLF71313T have an internal discharge N-channel FET switch on the V_{OUT} pin. When EN signal turns the main power FET to an off state, the N-channel switch turns on to discharge an output capacitor quickly.

Board Layout

All traces should be as short as possible to minimize parasitic inductance effects. Wide traces for V_{IN}, V_{OUT}, and GND will help reduce signal degradation and parasitic effects during dynamic operation as well as improve the thermal performance at high load current.

PACKAGE OUTLINE


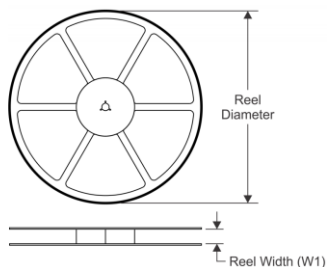
Dimensional Ref.			
REF.	Min.	Nom.	Max.
A	0.300	0.350	0.400
A1	0.075	0.100	0.125
A2	0.225	0.250	0.275
D	0.955	0.970	0.985
E	0.955	0.970	0.985
D1	0.450	0.500	0.550
E1	0.450	0.500	0.550
b	0.200	0.250	0.300
e	0.500 BSC		
SD	0.250 BSC		
SE	0.250 BSC		
Tol. of Form&Position			
aaa	0.10		
bbb	0.10		
ccc	0.05		
ddd	0.05		

Notes

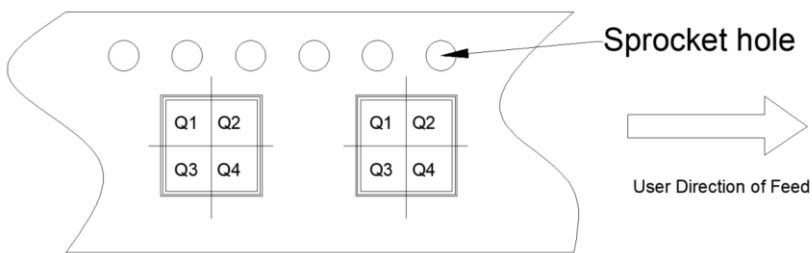
1. ALL DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.

TAPE AND REEL INFORMATION

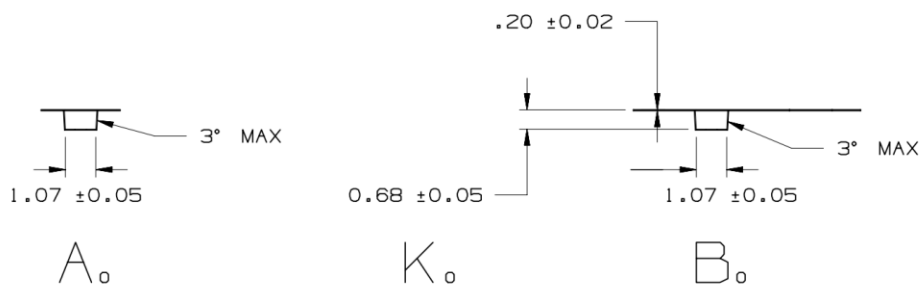
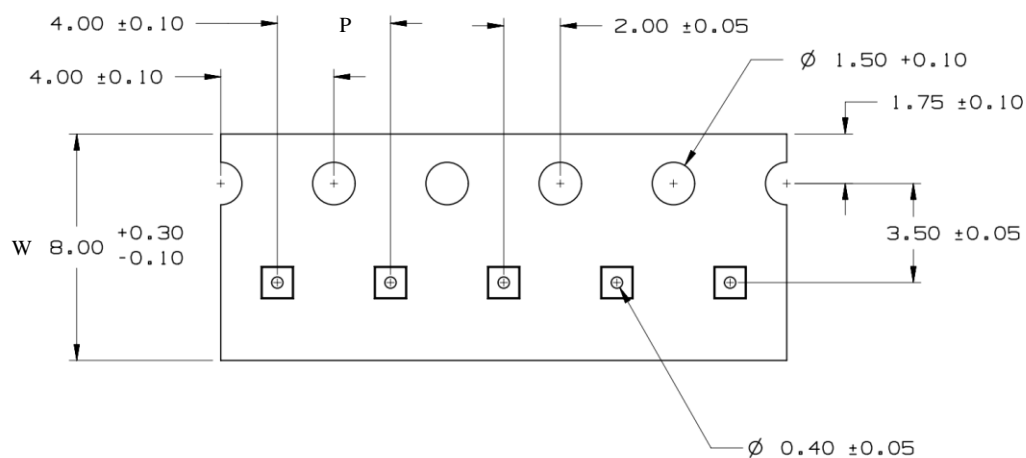
REEL DIMENSIONS



QUADRANT ASSIGNMENTS PIN 1 ORIENTATION TAPE



TAPE DIMENSIONS



Device	Package	Pins	SPQ	Reel Diameter(mm)	Reel Width W1	A0	B0	K0	P	W	Pin1
GLF71310T	WLCSP	4	3000	180	9	1.07	1.07	0.68	4	8	Q1
GLF71311T	WLCSP	4	3000	180	9	1.07	1.07	0.68	4	8	Q1
GLF71312T	WLCSP	4	3000	180	9	1.07	1.07	0.68	4	8	Q1
GLF71313T	WLCSP	4	3000	180	9	1.07	1.07	0.68	4	8	Q1

Remark:

A0: Dimension designed to accommodate the component width

B0: Dimension designed to accommodate the component length

C0: Dimension designed to accommodate the component thickness

W: Overall width of the carrier tape

P: Pitch between successive cavity centers

SPECIFICATION DEFINITIONS

Document Type	Meaning	Product Status
Target Specification	This is a target specification intended to support exploration and discussion of critical needs for a proposed or target device. Spec limits including typical, minimum, and maximum values are desired, or target, limits. GLF reserves the right to change limits at any time without warning or notification. A target specification in no way guarantees future production of the device in question.	Design / Development
Preliminary Specification	This is a preliminary version of a product specification. The specification is still under internal review and subject to change. GLF reserves the right to change the specification at any time without warning or notification. A preliminary specification in no way guarantees future production of the device in question.	Qualification
Product Specification	This document represents the anticipated production performance characteristics of the device.	Production

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