

Integrated Load Switch with Deep Sleep Mode

Product Specification

DESCRIPTION

The GLF76321 / GLF76321T is an ultra-thin, ultra-efficient I_QSmart^{TM} load switch with an integrated deepsleep timer for wearables and IoT devices.

The /SRO pin enables a whole system to enter ultradeep sleep power conservation mode by disconnecting the system from the battery charge, with ultra-low standby current of 7nA typical. With the switch placed between a battery and system, this switch can help to significantly extend system battery life in mobile devices during shipping or periods of extended off time.

The part supports two methods for entering the deep sleep: supporting both user and interrupt initiated events. Deep sleep can be initiated or exited by either holding the SRO pin low for a predefined delay time (ideal for user control) or by providing a rising edge signal to the OFF pin (ideal for logic or interrupt control).

To exit the deep sleep, the user can hold down the /SRO pin to ground for 1.3 seconds, or simply connect a charger adapter to trigger the Wake pin.

The GLF76321 / GLF76321T helps to reduce power consumption with the best in class R_{ON} and a breakthrough on state $I_{\rm Q}$ of only 3nA typical when the switch is on.

The GLF76321 / GLF76321T integrated 1ms slew rate control can also enhance system reliability by mitigating bus voltage swings during switching events. Where uncontrolled switching can generate high inrush currents that result in voltage droop and/or bus reset events, the GLF slew rate control specifically limits inrush currents during turn-on to minimize voltage droop. The output discharge functions makes output voltage off quickly during the reset period.

The GLF76321 is available in 0.97mm x 1.47mm x 0.55mm wafer level chip scale package (WLCSP). The GLF76321T is ultra-thin: 0.35mm Typ, 0.4mm Max.

FEATURES

Ultra-Low I_{SD}: 7 nA Typ @ 3.6VBAT
 Ultra-Low I_Q: 3 nA Typ @ 3.6VBAT
 Low R_{ON}: 31 mΩ Typ @ 3.6VBAT

I_{OUT} Max : 2A

• Wide Input Range: 1.5V to 5.5V

6Vabs max

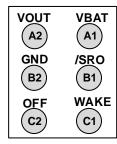
- Deep Sleep Mode by /SRO and OFF Pins
 Disconnect the downstream system from the
 battery source
- Integrated Delay Time(Hold Time) to Deep Sleep, 7 s
- Turn-Off Delay Time, 7 s
- Controlled Output Rise Time: 1ms at 3.6VBAT
- Integrated Output Discharge Switch When Disabled
- Operating Temperature Range: -40 to 85°C
- HBM: 6kV, CDM: 2kV
- Ultra-Small: 0.97mm x 1.47mm WLCSP
- Ultra-Thin on GLF76321T: **0.35mm Typ**., 0.4mm

APPLICATIONS

- Wearables
- IoT Devices
- Medical Devices

PACKAGE

VBAT	VOUT
(A1)	(A2)
/SRO	GND
(B1)	(B2)
WAKE	OFF
(C1)	(C2)



TOP VIEW

BOTTOM VIEW

0.97mm x 1.47mm x 0.55mm WLCSP 0.97mm x 1.47mm x 0.35mm Ultra-Thin WLCSP

DEVICE OPTIONS / PACKAGING INFORMATION

Part Number	Туре	Top Mark	/SRO Hold Time	Output Discharge	Package	Availability	Tape and Reel Packaging
GLF76320		SQ		NA	0.97mm x 1.47mm x 0.55mm WLCSP	On Request	
GLF76321	Deep Sleep after	SF	7 sec	85Ω 0.97mm x 1.47mm x 0.55mm WLCSP Released		3000 Pieces on 7 inch reel	
GLF76321T	7 sec	-		85Ω	0.97mm x 1.47mm x 0.35mm Ultra-Thin WLCSP	Released	on / monreel

APPLICATION DIAGRAM

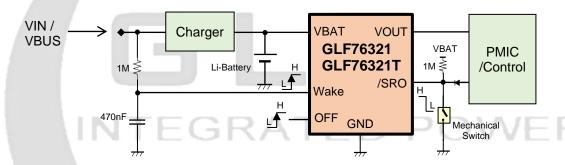


Figure 1. Typical Application with Standalone Charger IC

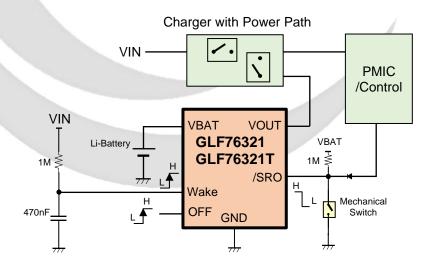


Figure 2. Typical Applications with Charger IC with Power Path and PMIC

FUNCTIONAL BLOCK DIAGRAM

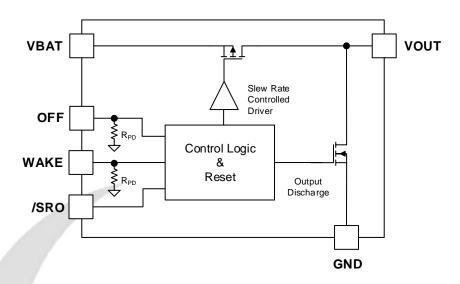


Figure 3. Functional Block Diagram

PIN CONFIGURATION

PIN DEFINITION

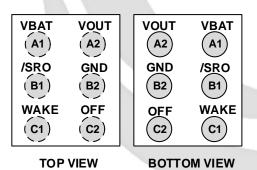


Figure 4. 0.97mm x 1.47mm x 0.55mm WLCSP 0.97mm x 1.47mm x 0.35mm Ultra-Thin WLCSP

Pin#	Name	Description
A1	VBAT	Switch Input. VBAT pin is connected to the positive input of an external battery.
A2	VOUT	Switch Output.
B1	/SRO	Reset Input or Power-On. Active Low. It needs an external pull-up resistor. It is typically connected to the center between an external pull-up resistor which is directly tied with the battery and a mechanical key button on a device.
B2	GND	Ground
C1	WAKE	System Wake Input. It is triggered by the rising edge signal to change the main switch from off to on-state. It has an internal pull-down resistance, $10M\Omega$ Typ. to keep the WAKE pin grounded. No need an external pull-down resistor.
C2	OFF	Main Switch Off Input. It is triggered by the rising edge signal to change the main switch from on to off-state. It has an internal pull-down resistance, $10M\Omega$ Typ. to keep the OFF pin grounded. No need an external pull-down resistor.

ABSOLUTE MAXIMUM RATINGS

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions; extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
VBAT, VOUT	Each Pin Voltage Range to GND		-0.3	6	V
/SRO, WAKE, OFF	Each Pin Voltage Range			6	V
Іоит	Maximum Continuous Switch Current			2	Α
P _D	Power Dissipation at T _A = 25°C			1.2	W
T _{STG}	Storage Junction Temperature			150	°C
T _A	Operating Temperature Range		-40	85	°C
θја	Thermal Resistance, Junction to Ambient			85	°C/W
FCD	Electrostatic Discharge Canability	Human Body Model, JESD22-A114	6		147
ESD	Electrostatic Discharge Capability	Charged Device Model, JESD22-C101	2		kV

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Max.	Unit
VBAT, VOUT	Supply Input and Output Voltage	1.5	5.5	V
/SRO, WAKE, OFF	Each Pin Voltage Range	0	5.5	V
TA	Ambient Operating Temperature	-40	+85	°C

ELECTRICAL CHRACTERISTICS

Values are at VBAT = 3.6V and $T_A = 25^{\circ}C$ unless otherwise noted.

Symbol	Parameter	Conditions			Тур.	Max.	Units
Basic Ope	ration						
Ιq	Quiescent Current	VBAT = /SRO = 3.6V, WAKW = OFF = GND I _{OUT} = 0mA, Load Switch = On			3		
	Charle Design Comment	VBAT=3.6V, VOUT=GND,	Load Switch = Off		7	20	nA
I _{SD}	Shut Down Current	VBAT=4.2V, VOUT=GND, Load Switch = Off			9		•
		VBAT=5.5V, I _{OUT} = 500mA	Ta=25°C		27		
		VBA1=3.5V, 1001= 300111A	Ta=85°C (1)		32		•
		VDAT 4.2V I 500 m A	Ta=25°C		29	31	
5	0 0 11	VBAT=4.2V, I _{OUT} = 500mA	Ta=85°C (1)		35		
R _{ON}	On-Resistance	VDAT 2 CV 1 500 A	Ta=25°C		31	33	mΩ
		VBAT=3.6V, I _{OUT} = 500mA	Ta=85°C (1)		37		1
		VBAT=3.0V, IouT= 300mA	Ta=25°C		34	36	
		VBAT=1.5V, IouT= 300mA	Ta=25°C		70		
Rosc	Output Discharge Resistance	VOUT = Off, IFORCE= 10mA		70	85	100	Ω
VIH	Input Logic High Voltage (2)	VBAT=1.5-5.5V		1.2			V
V_{IL}	Input Logic Low Voltage (2)	VBAT=1.5-5.5V				0.5	V
R _{PD}	Pull-down Resistance on OFF and WAKE	VBAT=5.5V			10	R	МΩ
Power On	(Load Switch Turn-On) and Deep	Sleep Timing by /SRO (1)				- 1 - 4	
tvon	Turn-On Delay Time(Hold Time)				1.3		
t _{Slp-Dly}	Delay Time(Hold Time) before Deep Sleep	VBAT=3.6V, $R_L = 150\Omega$, C_L	_ = 10uF		7		s
Power On	(Load Switch Turn-On) Timing by	WAKE (1)		/			
t_{dON}	Turn-On Delay				0.8		
t _R	VOUT Rise Time	VBAT=3.6V, R _L = 150Ω, C _L = 10uF			1		ms
ton	Turn-On Time (2)				1.8		
Power Off	(Load Switch Turn-Off) by OFF (1)			ı	1	I	
t _{SD}	Delay to Turn Off Load Switch				7		S
t _F	VOUT Fall Time	VBAT=3.6V, $R_L = 150 \Omega$, C	L = 10uF		1		ms
toff	Turn Off Time (3)				7		s

Notes:

- By design; characterized, not production tested.
 Input pins are /SRO, OFF, and WAKE.
- 3. $t_{ON} = t_{dON} + t_R$, $t_{OFF} = t_{SD} + t_F$

Integrated Load Switch with Deep Sleep Mode

TIMING DIAGRAMS AND INPUT CONDITION

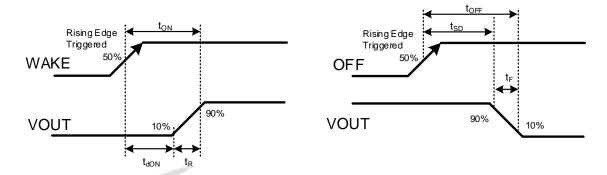


Figure 5. Power On by WAKE Pin

Figure 6. Power Off by OFF Pin

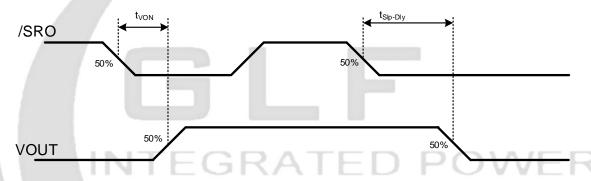


Figure 7. Power On and Deep Sleep by /SRO Pin

Table 1. Pin Default State With Input Power Source

Pin Name	/SRO	WAKE	OFF	VOUT
Default State	1	0	0	GND

Notes: 1=Logic High, 0=Logic Low, The VOUT=GND means the internal load switch is off.

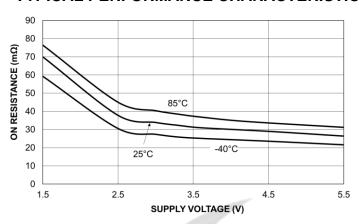
Table 2. Input Conditions and VOUT

Function	/SRO	WAKE	OFF	Delay Time(Hold time)	VOUT Action
Power-On	High to Low & Hold for tvon=1.3 s	Х	Х	t _{VON} =1.3 s	VOUT=VBAT
	High	Low to High Rising Edge Triggered	Х	t _{dON} =0.8 ms (2)	VOUT=VBAT
Power-Off	High to Low & Hold for $t_{Slp-Dly} = 7 \text{ s}$	Х	Х	t _{Slp-Dly} = 7 s	VOUT to GND
into Deep Sleep	High	Low	Low to High Rising Edge Triggered	t _{SD} = 7 s	VOUT to GND

Notes: 1. X = Don't Care

^{2.} The t_{dON} can be longer with an external capacitor on the WAKE pin due to a RC time-constant to the trigger level of rising edge.

TYPICAL PERFORMANCE CHARACTERISTICS



90 80 ON RESISTANCE (mQ) 70 $V_{IN} = 1.5V$ 60 50 40 $V_{IN} = 3.3V$ 30 $V_{IN} = 5.5V$ 20 10 0 -40 -15 85 T_J, JUNCTION TEMPERATURE (°C)

Figure 8. On-Resistance vs. Input Voltage

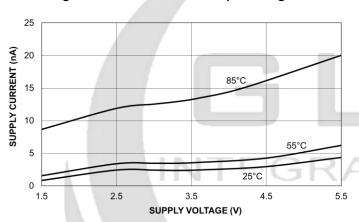


Figure 9. On-Resistance vs. Temperature

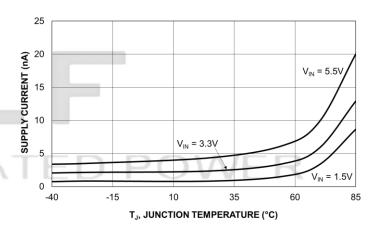


Figure 10. Quiescent Current vs. Input Voltage

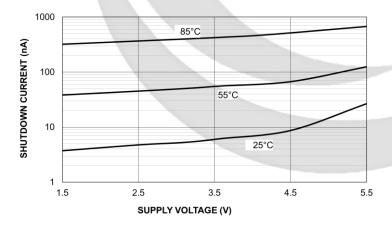


Figure 11. Quiescent Current vs. Temperature

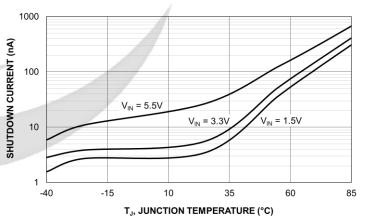


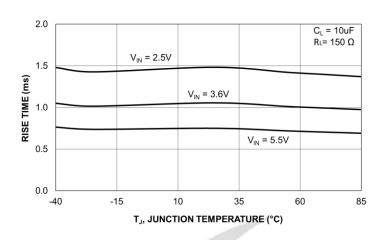
Figure 12. Shut Down Current vs. Input Voltage

Figure 13. Shut Down current vs. Temperature

POWER

GLF76321 / GLF76321T

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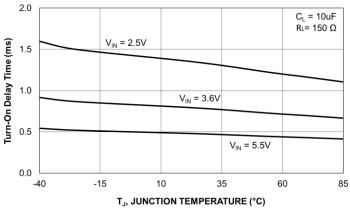


Figure 14. Vout Rise Time vs. Temperature

/SRO[2V/div]

/SRO[2V/div]

/SRO[2V/div]

/SRO[2V/div]

Figure 15. Turn-On Delay Time vs. Temperature

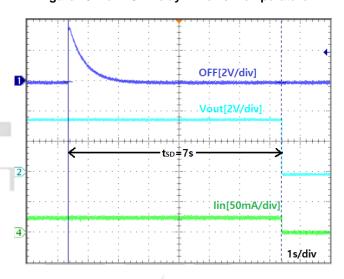


Figure 16. Delay time before Deep Sleep, tsip-Dly

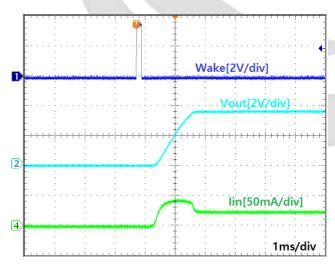


Figure 18. Turn-On Response $V_{IN}=3.6V$, $C_{IN}=10uF$, $C_{L}=10uF$, $R_{L}=150\Omega$

Figure 17. Turn-Off Response, tsD

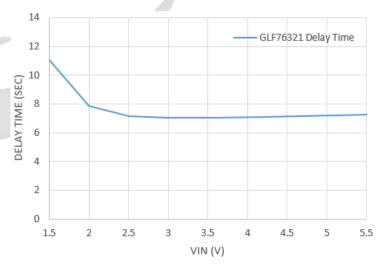


Figure 19. Delay Time of tsp and tsp-Dly vs. Input Voltage $C_{IN}=10uF, C_L=10uF, R_L=150\Omega$

Integrated Load Switch with Deep Sleep Mode

APPLICATION INFORMATION

INTEGRATED POWER

The GLF76321 / GLF76321T is an integrated load switch with the deep sleep mode which is optimized to significantly extend the battery life in mobile devices during long period of shipping or off time. Typical applications are shown in Fig.1 and Fig. 2.

Power On

There are two methods to enable the main switch of GLF76321 / GLF76321T to wake up the system. At this power-on process, the deep sleep function with /SRO pin is disabled. The Fig.20 shows the power-on mode by /SRO and WAKE pins. The output discharge switch

1) /SRO pin

When the main switch of GLF76321 / GLF76321T is turned off and a system is disabled, holding the /SRO pin low for the preset delay time or hold time, 1.3 seconds, turns on the main switch to wake up the downstream system.

2) WAKE pin

When a high signal is applied to the WAKE pin, the GLF76321 / GLF76321T turns on the main switch to connect the battery power to the downstream system. The Wake pin is initiated on a rising edge of a high signal. The t_{dON} of timing can be longer due to a RC time-constant to the trigger level of rising edge of WAKE pin. The WAKE pin has an internal pull-down resistance which is typically 10M Ohm to remain off state when no signal is asserted.

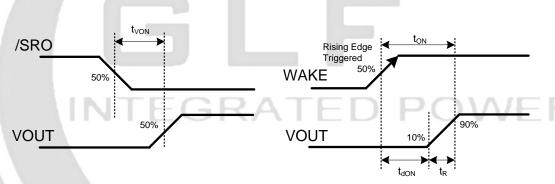


Figure 20. Power-On Mode by /SRO and WAKE

Deep Sleep Function

The GLF76321 / GLF76321T allows a mobile or wearable device to enter the deep sleep mode by disconnecting the downstream system from the battery charge and consuming 7nA typical standby current themselves. Two methods to activate the deep sleep mode are offered. The Fig. 21 shows how to enter the deep sleep mode by either /SRO or OFF pin. The output discharge switch of GLF76321 / GLF76321T is turned on to quickly bring VOUT down to GND when the main switch is turned off by both /SRO and OFF pins.

1) /SRO pin

When the main switch of GLF76321 / GLF76321T is turned on and then a downstream system operates, holding the /SRO pin low for the preset delay time or hold time turns off the main switch to cut off the supply power from the battery and the internal output discharge switch is turned on to make VOUT down to GND quickly. The GLF76321 / GLF76321T consumes ultra-low standby leakage current to keep the battery charge during the sleep mode. If the /SRO pin gets back to the high state within the preset delay time or hold time, the VOUT remains in on state. The /SRO pin needs a pull-up resistor to be tied to the battery to maintain the high state during the normal operation. It can be connected to an external key button on a device so that users can use it to enter the sleep mode as well as to reset the system. The preset delay or hold time, tsip-ply is 7 seconds.

2) OFF pin

When the OFF pin is triggered by a rising edge of the signal from low to high, the main switch of GLF76321 / GLF76321T is turned off in the preset delay time and enters the sleep mode. The output discharge switch is turned on to make VOUT down to GND quickly. Note that if the /SRO pin action of going low and high is detected within the preset delay time (tsd), the turn-off process is terminated and the VOUT remains in on state. To initiate

Integrated Load Switch with Deep Sleep Mode

the OFF pin again, the OFF pin needs to return to low and then a rising edge signal is asserted. The OFF pin has an internal pull-down resistor which is typically 10M Ohm to remain low state when no signal is asserted. The preset delay time, t_{SD} is 7 seconds.

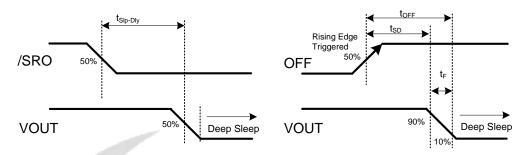


Figure 21. Deep Sleep Mode by /SRO and OFF

Input Priority

The GLF76321 / GLF76321T supports two different methods for turning on and off the main switch with /SRO, OFF, and WAKE pins. When two input pins are asserted at the same time or in any sequence, a higher priority input pin is chosen to be asserted and a lower priority input is ignored to avoid unnecessary conflicts.

Input	Priority (1 : Highest)
/SRO	MILL
WAKE	2
OFF	3

Table 3. Pin Priority

Output Discharge Function

The GLF76321 / GLF76321T has an internal discharge switch on VOUT. It is activated to discharge an output capacitor quickly when the main switch is turned off. During the sleep mode, the discharge switch remains in the on state holding the VOUT to GND. When the main switch is enabled, the output discharge switch is turned off.

Input Capacitor

A 0.1uF capacitor is recommended to be placed close to the VBAT pin to reduce the voltage drop on the input power rail caused by transient inrush current at start-up. A higher input capacitor value can be used to further attenuate the input voltage drop.

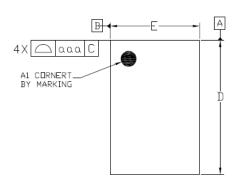
Output Capacitor

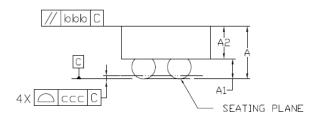
A 0.1uF output capacitor is recommended to mitigate voltage undershoot on the output pin when the switch is turned off. Undershoot can be caused by parasitic inductance from board traces or intentional load inductances. If load inductances exist, use of an output capacitor can improve output voltage stability and system reliability. The Cout capacitor should be placed close to the VOUT and GND pins.

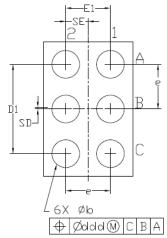


Integrated Load Switch with Deep Sleep Mode

PACKAGE OUTLINE (GLF76321)





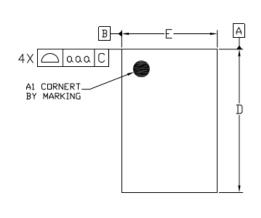


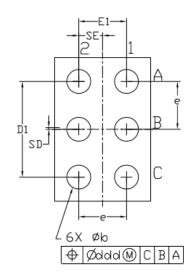
	Dimens	ional R	ef.			
REF.	Min.	Nom.	Max.			
Α	0.500	0.550	0.600			
A1	0.225	0.250	0.275			
A2	0.275	0.300	0.325			
D	1.460	1.470	1.485			
Е	0.960	0.970	0.985			
D1	0.950	1.000	1.050			
E1	0.450	0.500	0.550			
Ь	0.260	0.310	0.360			
е	0	.500 BS	С			
SD	0	.000 BS	C			
SE	0	.250 BS	C			
To	ol, of Fo	rm&Pos	sition			
999		0.10				
bbb		0.10				
333		0.05				
ddd		0.05				

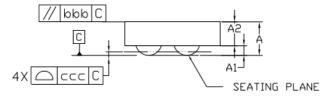
Notes

- 1, ALL DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
- 2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.

ULTRA-THIN PACKAGE OUTLINE (GLF76321T)







Dimensional Ref.							
REF.	Min.	Nom.	Max.				
Α	0.300	0.350	0.400				
A1	0.075	0.100	0.125				
A2	0.225	0.250	0.275				
D	1.460	1.470	1.485				
Ε	0.960	0.970	0.985				
D1	0.950	1.000	1.050				
E1	0.450	0.500	0.550				
Ь	0.210	0.250	0.290				
е	0	.500 BS	C				
SD	0	.000 BS	C				
SE	0	.250 BS	C				
Tol. of Form&Position							
aaa		0.10					
bbb		0.10					
ccc		0.05					
ddd		0.05					

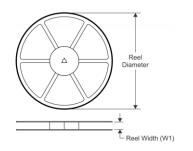
Notes

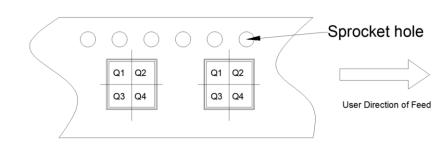
- 1. AU DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
- 2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.

TAPE AND REEL INFORMATION

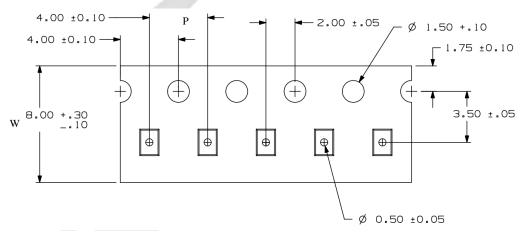
REEL DIMENSIONS

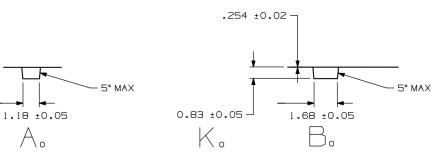
QUADRANT ASSIGNMENTS PIN 1 ORIENTATION TAPE





TAPE DIMENSIONS





Device	Package	Pins	SPQ	Reel Diameter(mm)	Reel Width W1	Α0	В0	K0	Р	w	Pin1
GLF76321	WLCSP	6	3000	180	9	1.18	1.68	0.83	4	8	Q1

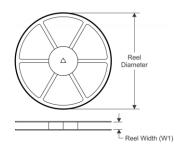
Remark:

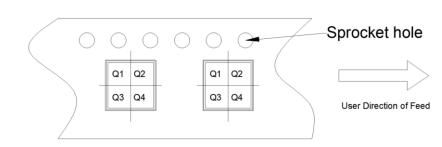
- A0: Dimension designed to accommodate the component width
- B0: Dimension designed to accommodate the component length
- C0: Dimension designed to accommodate the component thickness
- W: Overall width of the carrier tape
- P: Pitch between successive cavity centers

TAPE AND REEL INFORMATION

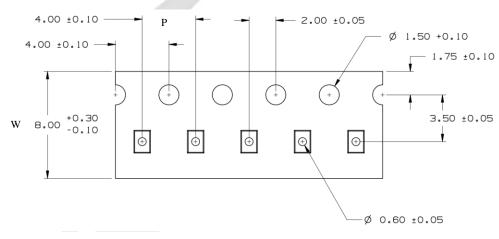
REEL DIMENSIONS

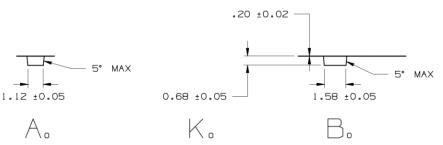
QUADRANT ASSIGNMENTS PIN 1 ORIENTATION TAPE





TAPE DIMENSIONS





Device	Package	Pins	SPQ	Reel Diameter(mm)	Reel Width W1	Α0	В0	K0	Р	w	Pin1
GLF76321T	WLCSP	6	3000	180	9	1.12	1.58	0.68	4	8	Q1

Remark:

- A0: Dimension designed to accommodate the component width
- B0: Dimension designed to accommodate the component length
- C0: Dimension designed to accommodate the component thickness
- W: Overall width of the carrier tape
- P: Pitch between successive cavity centers



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SPECIFICATION DEFINITIONS

Document Type	Meaning	Product Status
Target Specification	This is a target specification intended to support exploration and discussion of critical needs for a proposed or target device. Spec limits including typical, minimum, and maximum values are desired, or target, limits. GLF reserves the right to change limits at any time without warning or notification. A target specification in no way guarantees future production or producability of the device in question.	Design / Development
Preliminary Specification	This is a draft version of a product specification. The specification is still under internal review and subject to change. GLF reserves the right to change the specification at any time without warning or notification. A preliminary specification in no way guarantees future production or producability of the device in question.	Qualification
Product Specification	This document represents the anticipated production performance characteristics of the device.	Production

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