

### **GLF74139**

# 4.5 A Power Mux Switch with Auto & Manual Input Selection

#### **DECRIPTION**

The evaluation board EV014 features the GLF74139 is a fully integrated power path switch with the automatic and manual selection function. The GLF74139 offers an industry leading true reverse current blocking (TRCB) function to protect input sources when the VOUT increase higher than VIN abnormally.

The EN pin can be used along with the SEL pin to control two integrated main FETs of the GLF74139. By the combination of these two pins, one of input source selection modes is set to provide power to downstream system seamlessly.

The automatic selection mode chooses a higher input voltage source between two inputs. In the manual selection mode, one of input sources is connected to downstream

#### **FEATURES**

- Two-Input and Single-Output Power Multiplexer Switch
- Automatic and Manual Input Selection Modes
- True Reverse Current Blocking on Each Channel
- Supply Voltage Range:2.0 V to 5.5 V
- $R_{ON} = 20 \text{ m}\Omega$  Typ. at 5.5  $V_{IN1}$  or  $V_{IN2}$
- 4.5 A Continuous Output Current Capability Per Channel
- Ultra-Low I<sub>Q</sub>: 4 μA Typ at 5.5 V<sub>IN</sub>
- Ultra-Low I<sub>SD</sub>: 30 nA Max at 5.5 V<sub>IN</sub>
- Smart Control Pins

I<sub>EN</sub> and I<sub>SEL</sub>: 10 nA Typ at V<sub>EN</sub> or V<sub>SEL</sub>

 $> V_{IH}$ 

 $R_{EN}$  and  $R_{SEL}$ : 500 k $\Omega$  Typ

- HBM: 6 KV, CDM: 2 kV
- 1.27 mm x 1.67 mm, 12 Bump Wafer Level Chip Scale Package



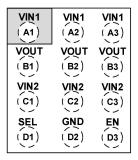
# **PRODUCT TABLE**

Eval Board Ordering Info	Part Number	R <sub>ON</sub> (Typ.) @ 5.5V <sub>IN</sub>	EN & SEL Activity
EV014-GLF74139	GLF74139	20 mΩ	High

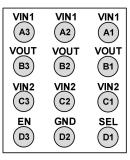
# **EVALUATION BOARD & DEVICE PACKAGE**



#### **PIN CONFIGURATION**



**TOP VIEW** 



**BOTTOM VIEW** 

#### **PIN DEFINITION**

Pin#	Name	Description	
A1, A2, A3	VIN1	Switch Input 1. Supply Voltage	
B1, B2, B3	VOUT	Switch Output	
C1, C2, C3	VIN2	Switch Input 2. Supply Voltage	
D1	SEL	Input Source Selection. Do not leave the SEL pin floating.	
D2	GND	Ground	
D3 EN		Enable to control the switch. Do not leave the EN pin floating.	



### **QUICK START GUIDE**

The evaluation board EV014 is easy to set up to evaluate the performance of GLF74139.

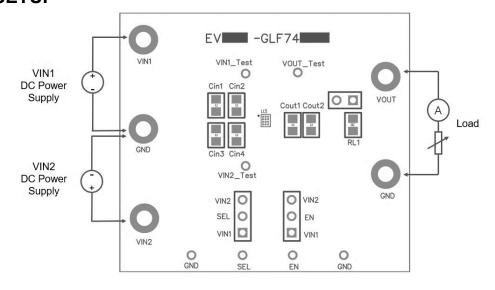
- 1. Preset the input power supply to the desired voltage between 2.0 V to 5.5 V.
- 2. The load resistor, RL1= 499  $\Omega$ , has been populated on the top of the PCB board. Short the jumper to use the RL1 or RL2 which is not populated. To increase the output current, connect an electronic load to VOUT and GND. The output current for the GLF74139 is rated for 4.5 A maximum output continuous current per each channel. Please ensure this absolute maximum is not exceeded.
- Connect the positive and negative terminals of the input power supply to VIN and GND respectively. VIN1\_Sense, VIN2\_Sense, and VOUT\_Sense can be used for measurement point.
- The input source selection function is set by the combination of SEL and EN. See Table 1 below. The SEL pin and the EN pin is connected to one of Input sources by J2 and J1 respectively. Note

   Do not leave the SEL and EN pins floating.
- 5. Turn on the input power supply.

SEL	EN	Function	VOUT
0	0	Both switches are off.	High-Z
0	O Auto-Input selection. VOUT is connected to a higher input source automatically.		Higher Input between VIN1 and VIN2
1 0 Only VIN1 is se		Only VIN1 is selected.	VIN1
1 1 Only VIN2 is selected.		Only VIN2 is selected.	VIN2

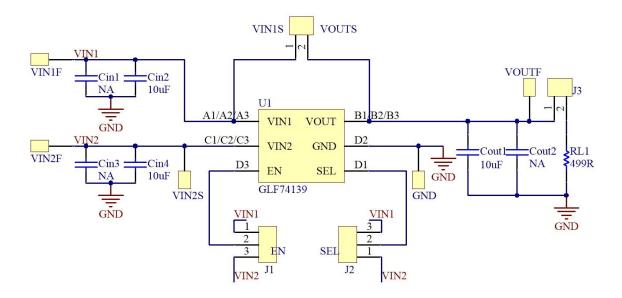
Table 1. Truth Table of Input Source Selection

### **TEST SETUP**





# **SCHEMATIC**



# **BILL OF MATERIALS**

Qty	Reference	Value	Part Description	Manufacturer/Part Number
1	U1	GLF74139	GLF74139	GLF Integrated Power
2	Cin2, Cin4	10 μF	Cap., X5R, 25V, 10% 0805	YAGEO CC0805KKX5R8BB106
1	Cout1	10 μF	Cap., X5R, 25V, 10% 0805	YAGEO CC0805KKX5R8BB106
1	Rout1	499 Ω	Output Resistor	YAGEO RC0805FR-07499RL
	C1, C2, Cout2	-	-	Not populated on the top
	RL2	-	Load Resistor	Not populated on the bottom
3	JP1-3	Jumper	Jumper	



# PRINTED CIRCUIT BOARD LAYOUT

Fig 1. Top Layer

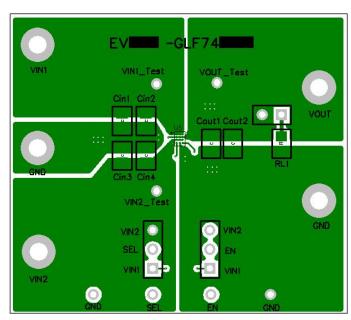
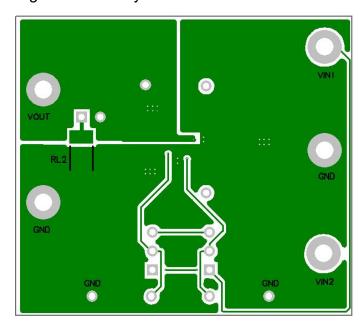


Fig 2. Bottom Layer



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