GLF4033

13 V, 4 A Power Mux IC with Manual Input Source Selection

Product Specification

DESCRIPTION

The GLF4033 is an integrated power multiplexer IC featuring dual independent power switches connected to a single output, enabling seamless transitions between two input power sources. The device supports a manual selection mode, configurable via the logic input pins S1 and S2. These pins allow system designers to manually select VIN1 only or VIN2 or and disable both switches.

The GLF4033 features low conduction resistance, enabling robust 4 A continuous current handling capability per channel. The device incorporates advanced cross-conduction protection that actively prevents current flow between input sources, maintaining isolation regardless of which power supply is active. The GLF4033 is ideally suited for power systems requiring an internal backup power supply.

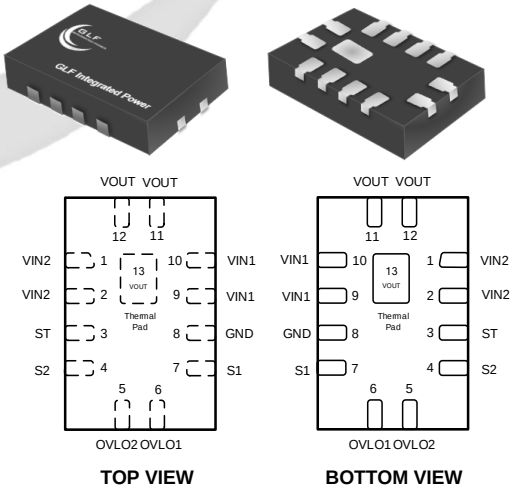
FEATURES

- Two-Input and Single-Output Power Multiplexer IC
- Manual Input Selection Mode
- Wide Input Range
  - VIN1 & VIN2 = 3 V to 13 V
- I_{OUT} Max: 4 A Per Channel, VIN1 and VIN2
- Low R_{ON}: 27 mΩ Typ.
- Low Quiescent Current, I_Q
  - 44 µA Typ. at V_{IN1} & V_{IN2} = 3 V
  - 56 µA Typ. at V_{IN1} & V_{IN2} = 5 V
  - 76 µA Typ. at V_{IN1} & V_{IN2}=13 V
- Low Stand-by Current, I_{SD}
  - 11 µA Typ. at V_{IN1} & V_{IN2} = 3 V
  - 14 µA Typ. at V_{IN1} & V_{IN2} = 5 V
  - 17 µA Typ. at V_{IN1} & V_{IN2}=13 V
- No Cross Conduction Between Two Input Sources
- Programmable Over-Voltage Protection
- Thermal Shutdown Protection
- State Indication Function
- Operating Temperature Range
  - - 40 °C to 85 °C

APPLICATIONS

- Power System with Backup Power
- Communication / Network System
- Security and Tracking System

PACKAGE



2 mm x 3 mm, QFN-13L

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PRODUCT INFORMATION

Part Number	Top Mark	R_{ON}	I_{OUT}	Package
GLF4033 - Q47	DX	27 mΩ	4 A	2 mm x 3 mm, QFN-13L

FUNCTIONAL BLOCK DIAGRAM

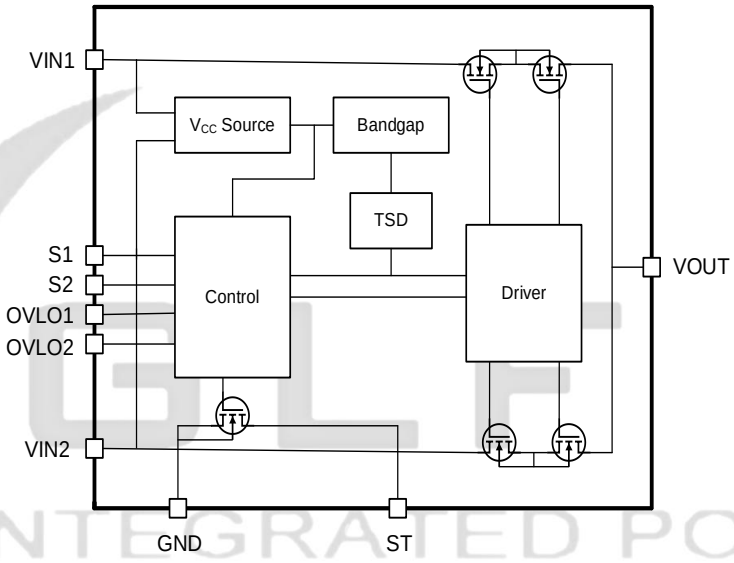

Figure 1. Functional Block Diagram

PIN CONFIGURATION

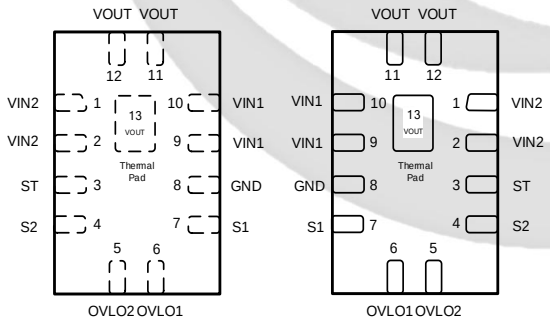

Figure 2. Package: 2 mm x 3 mm QFN-13L

PIN DEFINITION

Pin No	Name	Description
1, 2	VIN2	IC Input 2
3	ST	State indication
4	S2	Control logic input. Do not leave the S2 pin floating.
5	OVLO2	Programmable OVP for channel 2. Tie the OVLO2 pin to GND can disable OVP function
6	OVLO1	Programmable OVP for channel 1. Tie the OVLO1 pin to GND can disable OVP function
7	S1	Control logic input. Do not leave the S1 pin floating.
8	GND	Ground
9, 10	VIN1	IC Input 1
11,12, 13	VOUT	IC Output

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ABSOLUTE MAXIMUM RATINGS

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions; extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{IN1}, V_{IN2}, V_{OUT}	VIN1, VIN2, VOUT Pin Voltage		- 0.3	14	V
V_{S1}, V_{S2}, V_{ST} V_{OVLO1}, V_{OVLO2}	Control Pin Voltage		- 0.3	6	V
I_{OUT}	Continuous Output Current			4	A
T_J	Maximum Junction Temperature			150	°C
T_{STG}	Storage Temperature		- 65	150	°C
T_A	Ambient Operating Temperature Range		- 40	85	°C
θ_{JA}	Thermal Resistance, Junction to Ambient			60	°C/W
ESD	Electrostatic Discharge Capability	Human Body Model, JESD22-A114	2		kV
		Charged Device Model, JESD22-C101	1		

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Max.	Unit
V_{IN1}, V_{IN2}	VIN1, VIN2 Supply Voltage	3	13	V
V_{ST}	ST Pin External Pull-up Voltage		5	V

ELECTRICAL CHARACTERISTICS

T_A = 25 °C. Unless otherwise noted

Symbol	Parameter	Conditions		Min	Typ	Max	Units
Basic Operation							
I_{STBY_VIN1}	VIN1 Standby Current	V_{OUT} = V_{IN2}, I_{OUT} = 0 mA, V_{IN1} = 3 V, V_{IN1} > V_{IN2}			43	70	µA
		V_{OUT} = V_{IN2}, I_{OUT} = 0 mA, V_{IN1} = 5 V, V_{IN1} > V_{IN2}			55	80	
		V_{OUT} = V_{IN2}, I_{OUT} = 0 mA, V_{IN1} = 9 V, V_{IN1} > V_{IN2}			57	90	
		V_{OUT} = V_{IN2}, I_{OUT} = 0 mA V_{IN1} = 13 V, V_{IN1} > V_{IN2}	T_A = 25 °C		63	100	
			T_A = 85 °C (1)		67		
I_{STBY_VIN2}	VIN2 Standby Current	V_{OUT} = V_{IN1}, I_{OUT} = 0 mA, V_{IN2} = 3 V, V_{IN2} > V_{IN1}			45	70	
		V_{OUT} = V_{IN1}, I_{OUT} = 0 mA, V_{IN2} = 5 V, V_{IN2} > V_{IN1}			57	80	
		V_{OUT} = V_{IN1}, I_{OUT} = 0 mA, V_{IN2} = 9 V, V_{IN2} > V_{IN1}			59	90	
		V_{OUT} = V_{IN1}, I_{OUT} = 0 mA V_{IN2} = 13 V, V_{IN2} > V_{IN1}	T_A = 25 °C		65	100	
			T_A = 85 °C (1)		69		
I_{Q_VIN1}	VIN1 Quiescent Current	V_{OUT} = V_{IN1}, I_{OUT} = 0 mA, V_{IN1} = 3 V, V_{IN1} > V_{IN2}			44	55	
		V_{OUT} = V_{IN1}, I_{OUT} = 0 mA, V_{IN1} = 5 V, V_{IN1} > V_{IN2}			56	80	
		V_{OUT} = V_{IN1}, I_{OUT} = 0 mA, V_{IN1} = 9 V, V_{IN1} > V_{IN2}			64	90	
		V_{OUT} = V_{IN1}, I_{OUT} = 0 mA V_{IN1} = 13 V, V_{IN1} > V_{IN2}	T_A = 25 °C		76	110	
			T_A = 85 °C (1)		81		

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ELECTRICAL CHARACTERISTICS (CONTINUED)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
Basic Operation							
I_{Q_VIN2}	VIN2 Quiescent Current	$V_{OUT} = V_{IN2}$, I_{OUT} = 0 mA, V_{IN2} = 3 V, $V_{IN2} > V_{IN1}$			43	55	μA
		$V_{OUT} = V_{IN2}$, I_{OUT} = 0 mA, V_{IN2} = 5 V, $V_{IN2} > V_{IN1}$			56	80	
		$V_{OUT} = V_{IN2}$, I_{OUT} = 0 mA, V_{IN2} = 9 V, $V_{IN2} > V_{IN1}$			63	90	
		$V_{OUT} = V_{IN2}$, I_{OUT} = 0 mA, V_{IN2} = 13 V, $V_{IN2} > V_{IN1}$	T_A = 25 °C		75	110	
			T_A = 85 °C (1)		81		
I_{SD_VIN1}	VIN1 Shutdown Current	V_{OUT} = High-Z, V_{IN1} = 3 V, $V_{IN1} > V_{IN2}$			10		
		V_{OUT} = High-Z, V_{IN1} = 5 V, $V_{IN1} > V_{IN2}$			12		
		V_{OUT} = High-Z, V_{IN1} = 9 V, $V_{IN1} > V_{IN2}$			14	26	
		V_{OUT} = High-Z, V_{IN1} = 13 V, $V_{IN1} > V_{IN2}$	T_A = 25 °C		17	50	
			T_A = 85 °C (1)		19		
I_{SD_VIN2}	VIN2 Shutdown Current	V_{OUT} = High-Z, V_{IN2} = 3 V, $V_{IN2} > V_{IN1}$			11		
		V_{OUT} = High-Z, V_{IN2} = 5 V, $V_{IN2} > V_{IN1}$			13		
		V_{OUT} = High-Z, V_{IN2} = 9 V, $V_{IN2} > V_{IN1}$			14	26	
		V_{OUT} = High-Z, V_{IN2} = 13 V, $V_{IN2} > V_{IN1}$	T_A = 25 °C		17	50	
			T_A = 85 °C (1)		19		
I_{S1}, I_{S2}	S1 and S2 Pin Leakage	$V_{S1} = V_{S2}$ = 5 V			10		nA
I_{ST}	ST Pin Leakage	V_{ST} = 5 V			6		
R_{ON}	On-Resistance	V_{IN}= 3 V to 13 V, I_{OUT} = 200 mA	T_A = 25 °C		27	36	mΩ
			T_A = 85 °C (1)		32		
V_{OVP_TH}	OVP Set Threshold	OVLO pin voltage rising, Device turns off V_{IN} = 3 V to 13 V		0.9	1.02	1.2	V
	OVP Hysteresis				35		mV
t_{OVP}	OVP Response Time (1)	$V_{IN} > V_{OVLO}$ to V_{OUT} stop rising C_{IN} = 1 μF, C_{OUT} = Open, R_L = 500 Ω			8		μs
V_{TH}	S1, S2 Logic High Voltage	V_{IN} = 3 V to 13 V		0.9	1.02	1.2	V
	S1, S2 Hysteresis				35		mV
T_{SD}	Thermal Shutdown Protection (1)	Thermal Shutdown Threshold 20 °C Hysteresis			150		°C
Switching Characteristics (1)							
t_{dON}	V_{OUT} Turn-On Delay Time	C_{OUT} = 100 μF R_L = 150 Ω	V_{IN1} = 3 V		250		μs
			V_{IN1} = 5 V		190		
			V_{IN1} = 13 V		190		
t_R	V_{OUT} Rise Time		V_{IN1} = 3 V		430		
			V_{IN1} = 5 V		340		
			V_{IN1} = 13 V		310		
t_{dOFF}	V_{OUT} Turn-Off Delay Time		V_{IN1} = 3 V		710		
			V_{IN1} = 5 V		500		
			V_{IN1} = 13 V		170		
t_F	V_{OUT} Fall Time		V_{IN1} = 3 V		25		ms
			V_{IN1} = 5 V		22		
			V_{IN1} = 13 V		15		

Note: 1. By design; characterized, not production tested.

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APPLICATION DIAGRAM

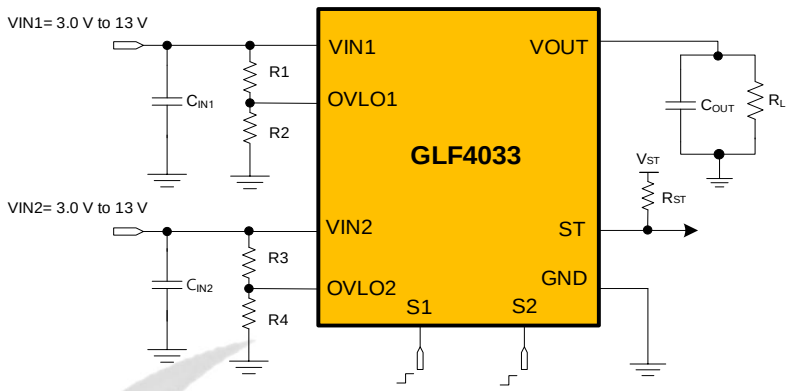

Figure 3. Programmable Over Voltage Protection

Notes: 1. VIN1 OVP trigger Voltage ≈ V_{OVP_TH} x (1 + R1 / R2), Recommended R2 ≤ 1 MΩ.
2. VIN2 OVP trigger Voltage ≈ V_{OVP_TH} x (1 + R3 / R4), Recommended R4 ≤ 1 MΩ.
3. V_{OVP_TH} of OVLO1 and OVLO2 = 1.02 V.
4. Recommended R_{ST} ≤ 1 MΩ and V_{ST} ≤ 5 V.

TRUTH TABLE AND TIMING DIAGRAM

S1	S2	VOUT	ST	Function
High	High	VIN1	High	VIN1 is selected
Low	High	VIN2	Low	VIN2 is selected
High	Low	High-Z	Low	Both channels are off

Notes: Input Logic High Voltage : ≥ 1.2 V
Input Logic Low Voltage : ≤ 0.85 V

Table 1. Input Source Selection Truth Table

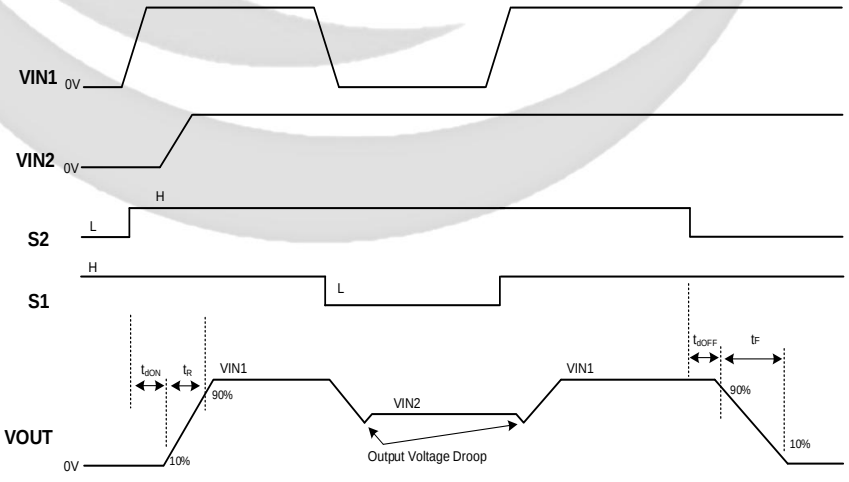

Figure 4. Timing Diagram
High : $V_{S1, S2} > V_{TH}$, Low : $V_{S1, S2} < V_{TH}$ - Hysteresis

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TYPICAL PERFORMANCE CHARACTERISTICS

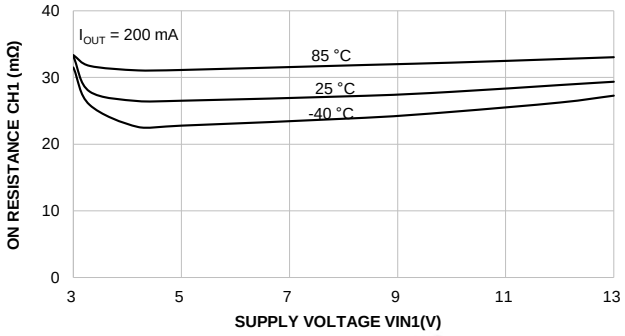

Figure 5. On-Resistance vs. Supply Voltage, Channel 1

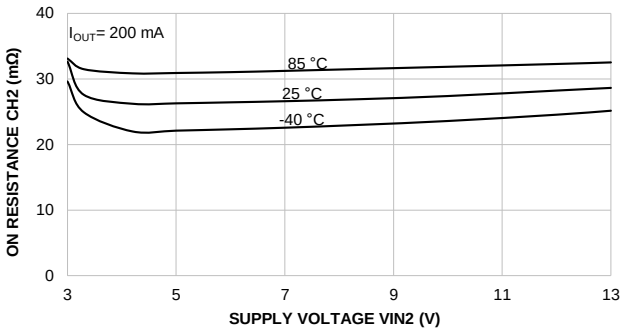

Figure 6. On-Resistance vs. Supply Voltage, Channel 2

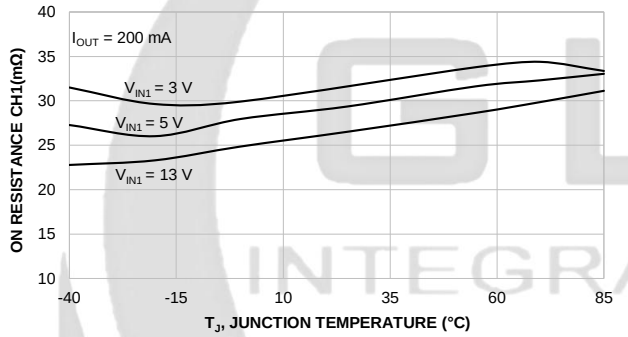

Figure 7. On-Resistance vs. Temperature, Channel 1

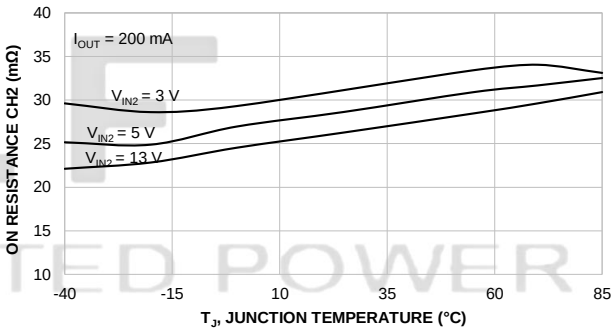

Figure 8. On-Resistance vs. Temperature, Channel 2

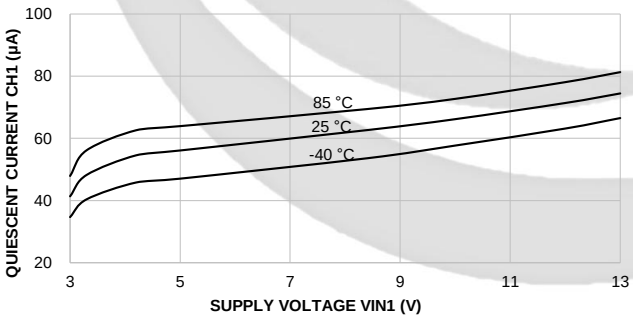

Figure 9. VIN1 Quiescent Current vs. Supply Voltage

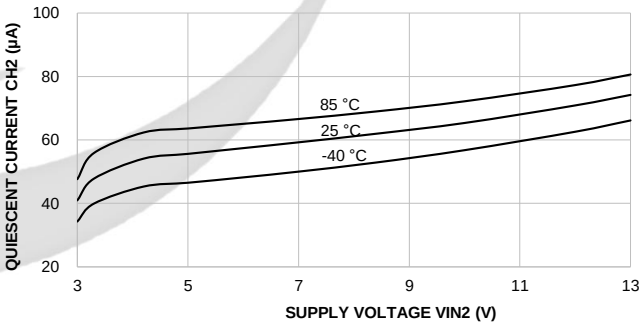

Figure 10. VIN2 Quiescent Current vs. Supply Voltage

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TYPICAL PERFORMANCE CHARACTERISTICS (CONTINUED)

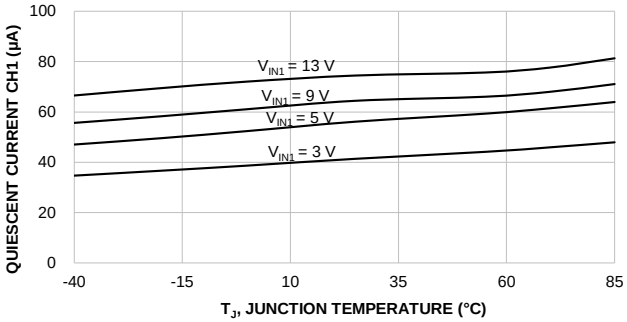

Figure 11. VIN1 Quiescent Current vs. Temperature

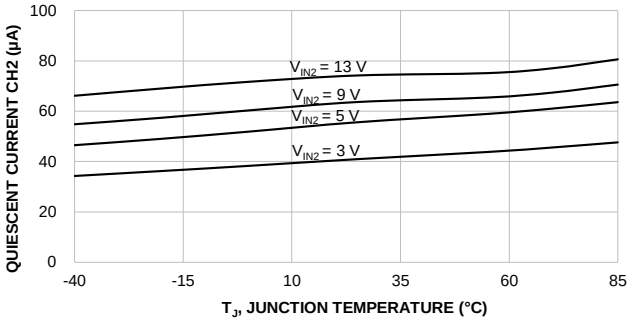

Figure 12. VIN2 Quiescent Current vs. Temperature

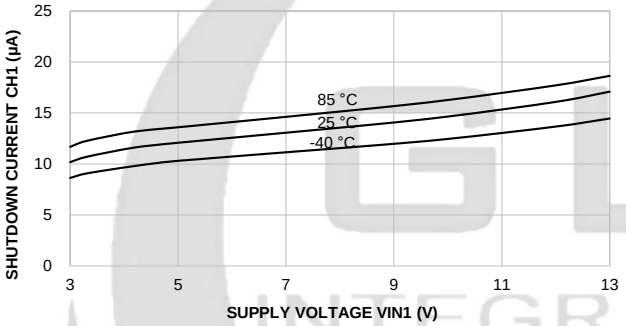

Figure 13. VIN1 Shutdown Current vs. Supply Voltage

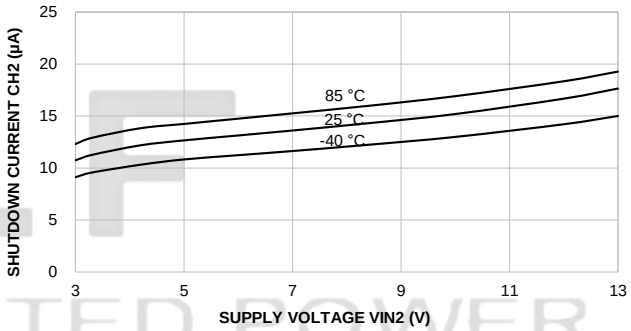

Figure 14. VIN2 Shutdown Current vs. Supply Voltage

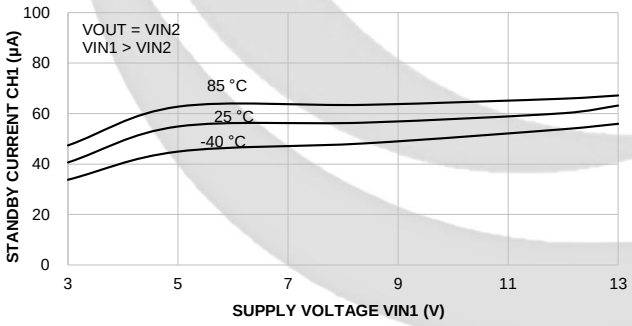

Figure 15. VIN1 Standby Current vs. Supply Voltage

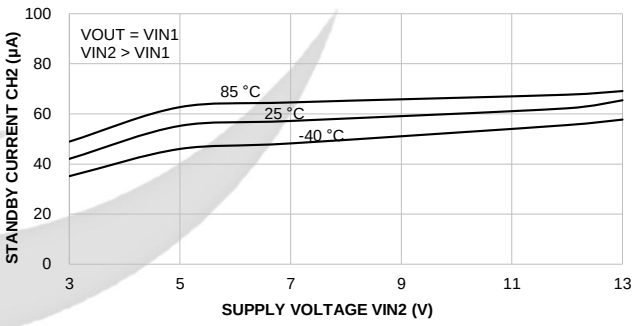

Figure 16. VIN2 Standby Current vs. Supply Voltage

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TYPICAL PERFORMANCE CHARACTERISTICS (CONTINUED)

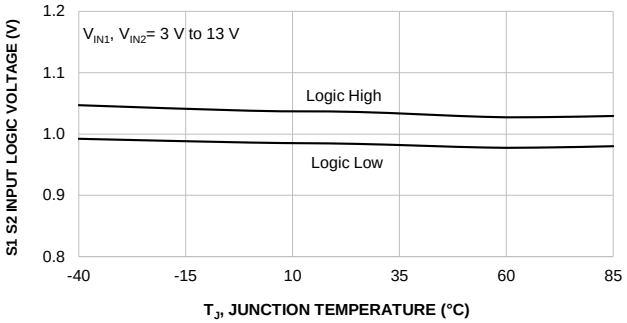

Figure 17. S1, S2 Input Logic Voltage vs. Temperature

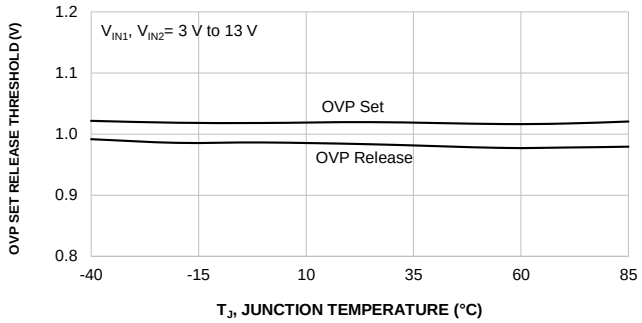

Figure 18. OVP Set and Release Threshold vs. Temperature

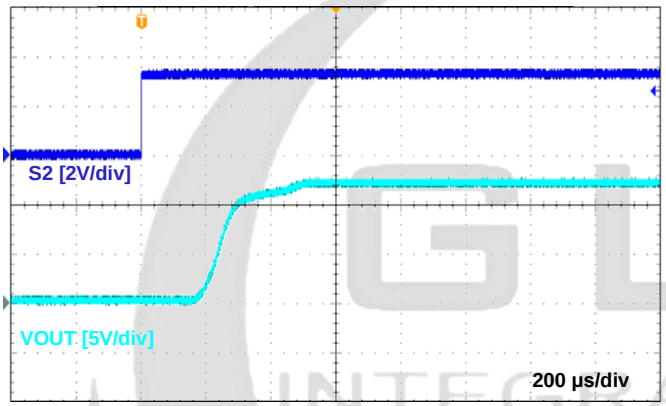

Figure 19. Turn-On Response, Channel 1
V_{IN1}=12 V, C_{OUT} =100 µF, R_L=150 Ω, S1=High

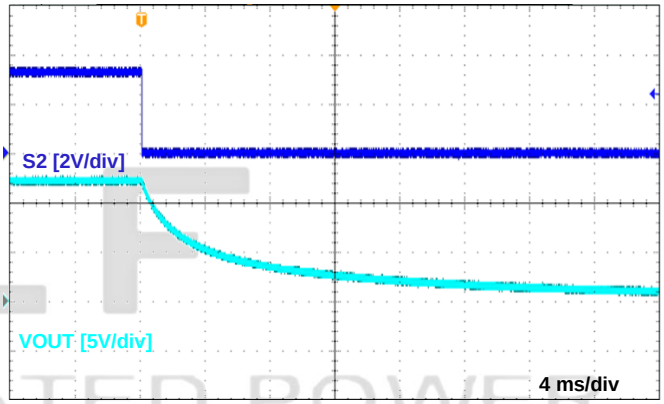

Figure 20. Turn-Off Response, Channel 1
V_{IN1}=12 V, C_{OUT} =100 µF, R_L=150 Ω, S1=High

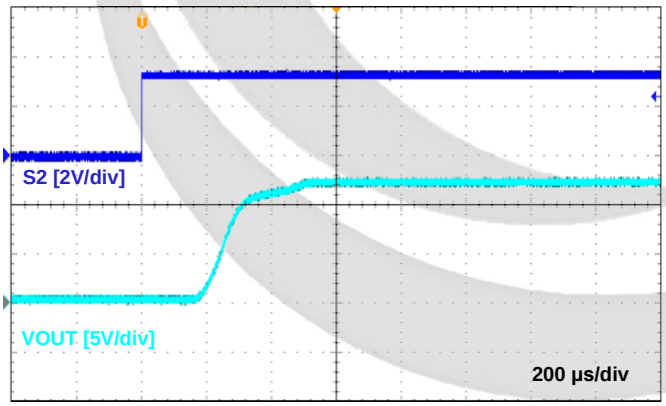

Figure 21. Turn-On Response, Channel 2
V_{IN2}=12 V, C_{OUT} =100 µF, R_L=150 Ω, S1=High to Low

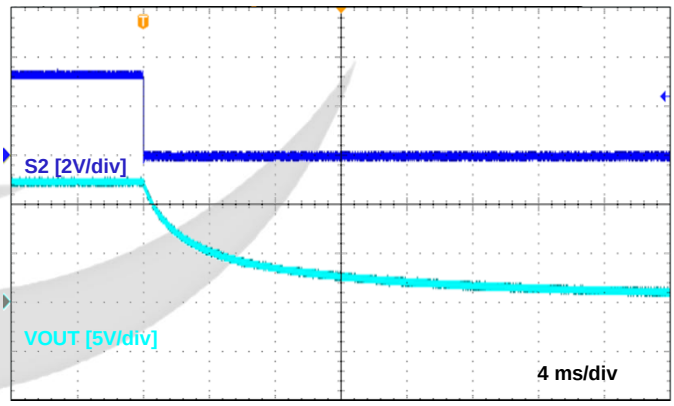

Figure 22. Turn-Off Response, Channel 2
V_{IN2}=12 V, C_{OUT} =100 µF, R_L=150 Ω, S1=High to Low

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TYPICAL PERFORMANCE CHARACTERISTICS (CONTINUED)

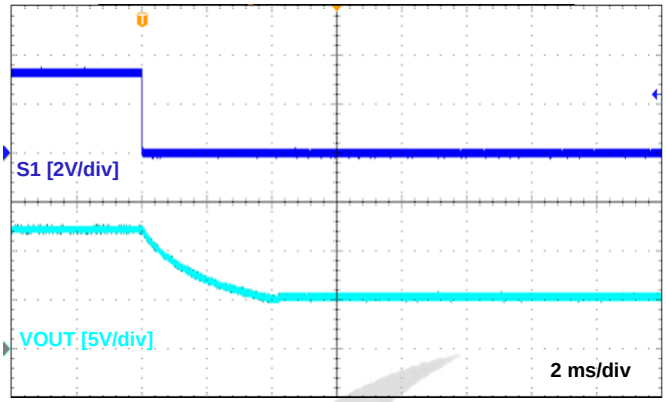

Figure 23. VOUT Switchover from 12 V to 5 V
V_{IN1}=12 V, V_{IN2}=5 V, C_{OUT}=100 µF, R_L=150 Ω, S2=High

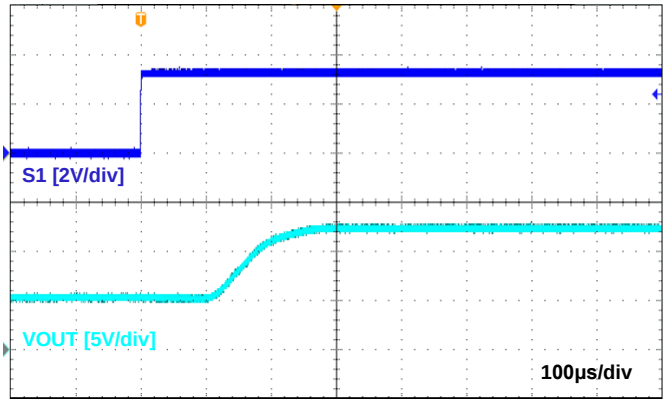

Figure 24. VOUT Switchover from 5 V to 12 V
V_{IN1}=12 V, V_{IN2}=5 V, C_{OUT}=100 µF, R_L=150 Ω, S2=High

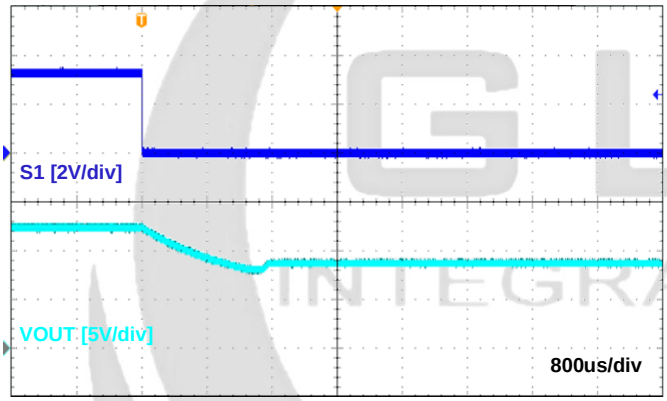

Figure 25. VOUT Switchover from 12 V to 8.4 V
V_{IN1}=12 V, V_{IN2}=8.4 V, C_{OUT}=100 µF, R_L=150 Ω, S2=High

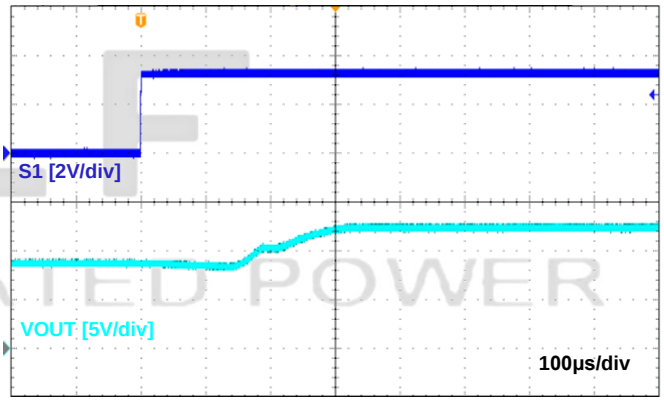

Figure 26. VOUT Switchover from 8.4 V to 12 V
V_{IN1}=12 V, V_{IN2}=8.4 V, C_{OUT}=100 µF, R_L=150 Ω, S2=High

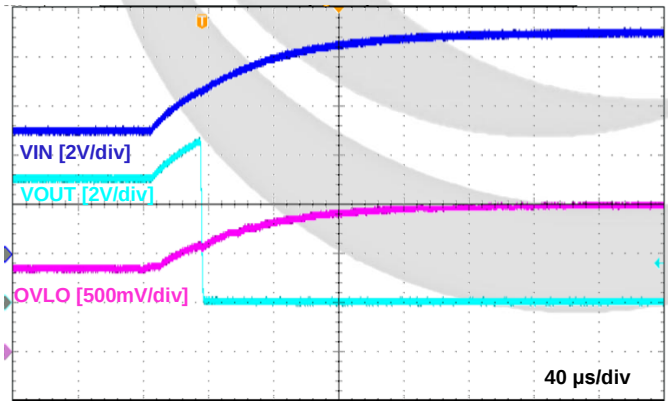

Figure 27. OVP Response
OVP Threshold=6.5 V V_{IN}, C_{OUT}=Open, R_L=500 Ω

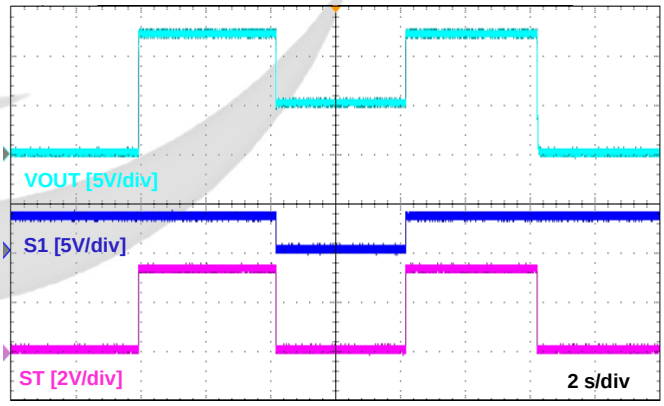

Figure 28. State (ST Pin) indication
V_{IN1}=12V, V_{IN2}=5 V, C_{OUT}=100 µF, R_L=150 Ω

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APPLICATION INFORMATION

The GLF4033 is a fully integrated power mux IC with symmetrical two channels and a fixed slew rate control to limit the inrush current during turn on in the input voltage range from 3 V to 13 V. It has very low on-resistance to reduce conduction loss. In the off state, it consumes very low leakage current to avoid unwanted standby current and save limited input power supply.

Input Source Selection

According to the state of S1 and S2 pins, the GLF4033 offers the VOUT connects to one input source. Do not leave both S1 and S2 pins floating.

S1	S2	VOUT	ST	Function
High	High	VIN1	High	VIN1 is selected
Low	High	VIN2	Low	VIN2 is selected
High	Low	High-Z	Low	Both channels are off

Table 2. Input Source Selection

State Indication

The ST pin is an open-drain output that should be pulled up to an external voltage for it to function properly. When GLF4033 uses VIN1 to power the output, the ST pin will be pulled high by an external voltage source. When GLF4033 uses VIN2 to power the output or both channels are disabled, the ST pin will be pulled low. During thermal shutdown, the ST pin will be pulled low, regardless of the channel used.

Over Voltage Lockout Protection

The GLF4033 utilizes an external resistor divider to provide programmable over-voltage protection (OVP) for both input power sources. For example, when VIN1 is selected as the output, if the rising voltage of VIN1 causes the OVLO1 pin voltage to exceed the V_{OVP_TH} threshold, the device will automatically switch the output to VIN2. However, if VIN2 is either unconnected or its voltage also exceeds the V_{OVP_TH} threshold at this moment, the device will shut down the output completely.

Output Voltage Droop at Switching Over

When the input source switches to another input source, the output voltage droop under switching conditions depends on the load resistance and output capacitance. The higher the load current during switching, the greater the output voltage droop. To mitigate the output voltage droop and ensure sufficient load current during switching, it is recommended to use a reasonably large output capacitor.

Board Layout

All traces should be as short as possible to minimize parasitic inductance effect. Wide traces for VIN, VOUT, and GND will help reduce signal degradation and parasitic effects during dynamic operations as well as improve the thermal performance at high load current.

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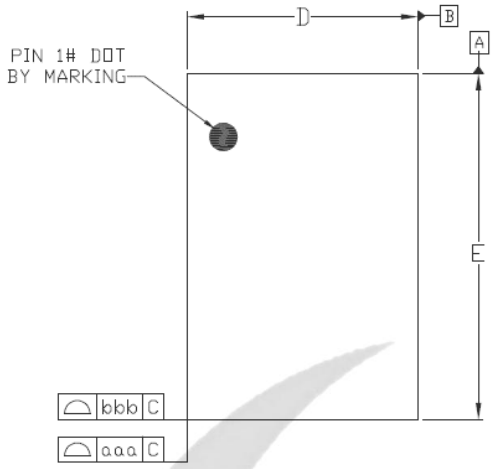
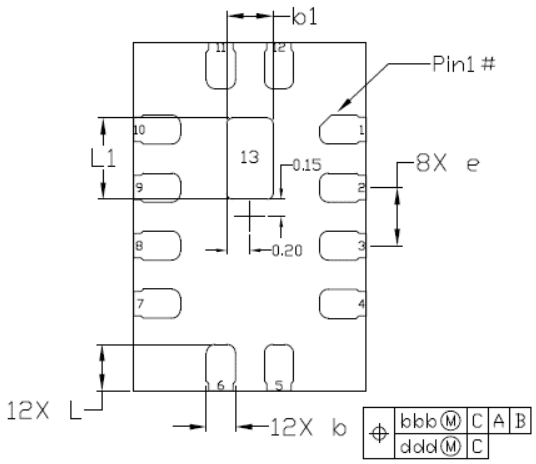
PACKAGE OUTLINE



TOP VIEW



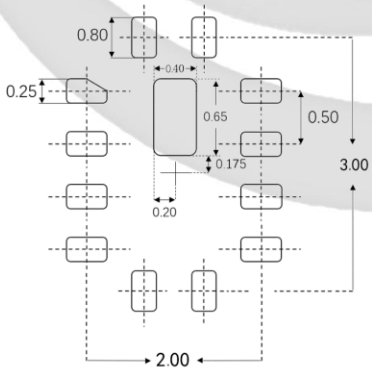
BOTTOM VIEW

SIDE VIEW

REF.	Dimensions Ref.		
	Min.	Nom.	Max.
A	0.500	0.550	0.600
A1	0.000	---	0.050
A3		0.152 Ref.	
D	1.950	2.000	2.050
E	2.950	3.000	3.050
b	0.200	0.250	0.300
b1	0.350	0.400	0.450
e		0.500 BSC	
L	0.350	0.400	0.450
L1	0.650	0.700	0.750
Tol. of Form & Position			
aaa		0.10	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	

Notes:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2018.
2. NX IS THE TOTAL NUMBER OF TERMINALS

Recommended Footprint



PACKAGING INFORMATION

Part Number	Package	Pins	Pitch	Top Mark	Moisture Sensitivity Level	Environmental Information
GLF4033-Q47	2mmx3mm QFN -13L	13	0.50mm	DX	MSL1	ROHS+HF

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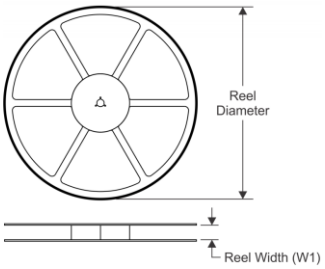
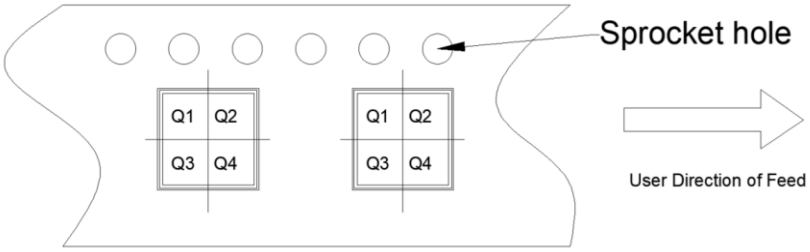
TAPE AND REEL INFORMATION

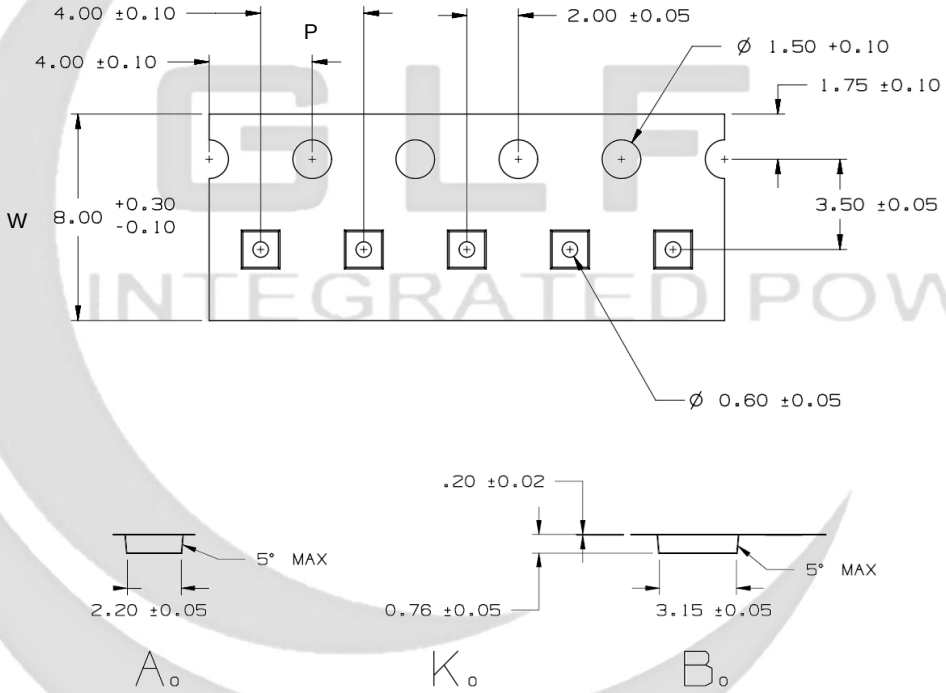
REEL DIMENSIONS



QUADRANT ASSIGNMENTS PIN 1 ORIENTATION TAPE



TAPE DIMENSIONS



Device	Package	Pins	SPQ	Reel Diameter (mm)	Reel Width W1	A0	B0	K0	P	W	Pin1
GLF4033-Q47	2mmx3mm QFN -13L	13	3000	180	9	2.20	3.15	0.76	4	8	Q1

Remark:

A0: Dimension designed to accommodate the component width

B0: Dimension designed to accommodate the component length

K0: Dimension designed to accommodate the component thickness

W: Overall width of the carrier tape

P: Pitch between successive cavity centers

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SPECIFICATION DEFINITIONS

Document Type	Meaning	Product Status
Target Specification	This is a target specification intended to support exploration and discussion of critical needs for a proposed or target device. Parameters including the typical, minimum, and maximum values are desired, or target. GLF reserves the right to change contents at any time without warning or notification. A target specification will not guarantee the future production of the device.	Design / Development
Preliminary Specification	This is a draft version of a product specification which is under internal review and subject to change. GLF reserves the right to change the specification at any time without warning or notification. A preliminary specification will not guarantee the future production of the device.	Qualification
Product Specification	This document represents the characteristics of the device.	Production

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