GLF4010, GLF4012

Ultra-low I_Q, Low Output Voltage Droop, 6 A Symmetrical Power Mux

Product Specification

DESCRIPTION

The GLF4010 and GLF4012 are ultra-low I_Q integrated power multiplexer IC with dual independent power switches connected to a single output pin to enable seamless transition between two input sources. The GLF4010 and GLF4012 feature symmetrical power FET characteristics. Channel 1 (VIN1) and channel 2 (VIN2) provide ultra-low conduction resistance to support 6 A continuous current capability. It is an ideal solution for a power system with an internal back up power source.

The GLF4010 and GLF4012 provide an automatic selection mode, a manual selection mode and VIN1 preference mode. The switching of these three modes is executed by combining the S1 and S2 pin settings. The S1 input pin has an internal threshold voltage to offer a preference to select the channel 1 (VIN1) power source. In the automatic input selection mode, the GLF4010 and GLF4012 automatically select a higher input voltage source between two input power sources.

The GLF4010 and GLF4012 prevent cross conduction current between two input sources. When VOUT is higher than VIN, the GLF4012 prevents the reverse current from the output to the input, no matter which input supply is applied.

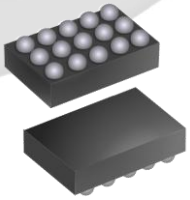
FEATURES

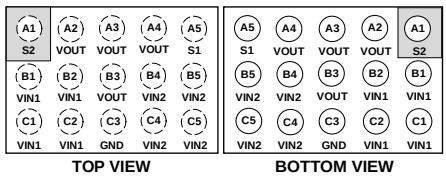
- Two-Input and Single-Output Power Multiplexer IC
- Auto & Manual & VIN1 Preference Selection Mode
- Wide Input Range: 1.5 V to 5.5 V
- Low R_{ON}
  - 15 mΩ Typ at 5.5 V_{IN}
- I_{OUT} Max: 6 A Per Channel, VIN1 and VIN2
- Ultra-low Quiescent Current
  - I_Q : 1.4 µA Typ at 5.5 V_{IN}
- Low Shutdown Current
  - I_{SD} : 1.0 µA Typ at 5.5 V_{IN}
- Reverse Current Blocking Protection: Only GLF4012
- Thermal Shutdown Protection
- Wide Operating Temperature Range: - 40 °C to 105 °C

APPLICATIONS

- Smart Door Lock
- Subsystem with Backup Power
- Multi-channel Power Management
- Communication / Network System

PACKAGE





TOP VIEW BOTTOM VIEW

1.17 mm x 1.97 mm x 0.55 mm WLCSP

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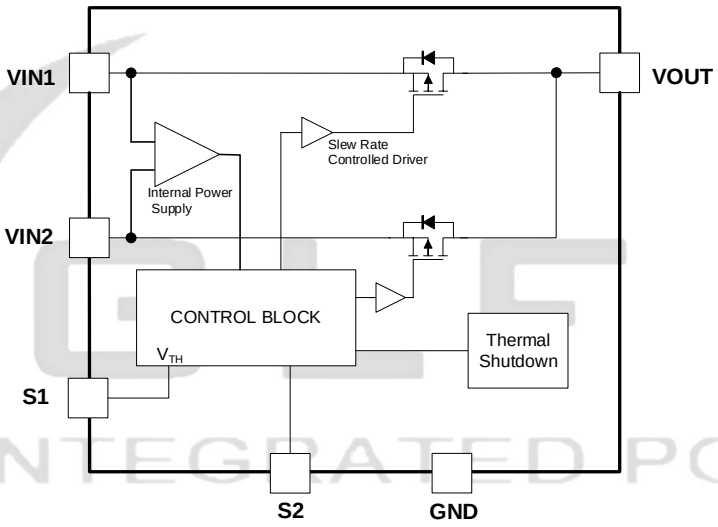
PRODUCT INFORMATION

Part Number	Top Mark	R_{ON} (Typ.)	I_{OUT} (Max)	Reverse Current Blocking	Output Discharge (Typ.)	Package	DS Status
GLF4010-SA7	IA	15 mΩ	6 A	NA	NA	1.17 mm x 1.97 mm x 0.55 mm WLCSP	Preliminary
GLF4011-SA7	IB			YES	100 Ω		On Request
GLF4012-SA7	IC			YES	NA		Product

FUNCTIONAL BLOCK DIAGRAM

GLF4010-SA7



GLF4012-SA7

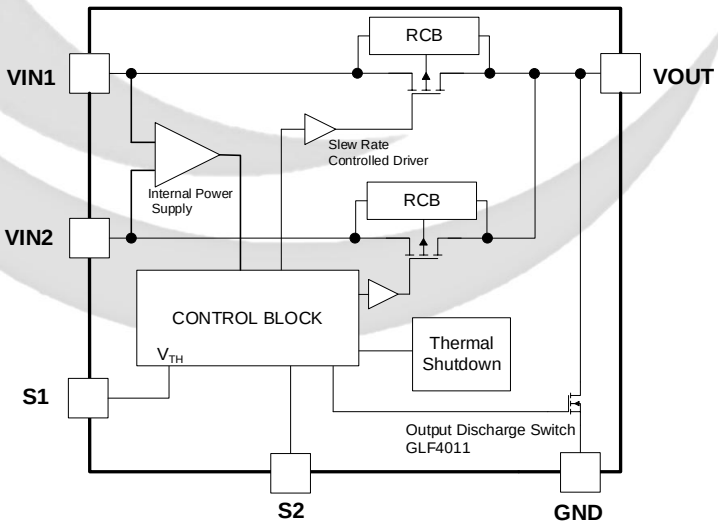


Figure 1. Functional Block Diagram

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PIN CONFIGURATION

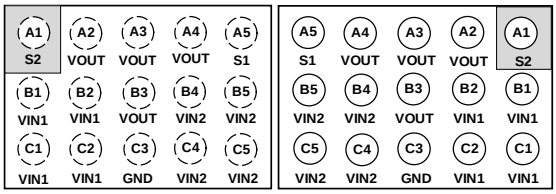

Figure 2. 1.17 mm x 1.97mm WLCSP

PIN DEFINITION

Pin #	Name	Description
B1, B2, C1, C2	VIN1	IC Input 1
A2, A3, A4, B3	VOUT	IC Output
B4, B5, C4, C5	VIN2	IC Input 2
C3	GND	Ground
A5	S1	Select Pin between VIN1 and VIN2 While S2 pin fixed high, if S1 is higher than V_{TH}, VIN1 is selected. Vice versa, VIN2 is chosen if S1 is low.
A1	S2	Manual or automatic selection mode Pin

ABSOLUTE MAXIMUM RATINGS

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions; extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{IN1}, V_{IN2}, V_{OUT}	Each Pin Voltage Range to GND		- 0.3	6	V
V_{S1}, V_{S2}	Control Pin Voltage		- 0.3	6	V
I_{OUT}	Continuous Output Current	VIN1 or VIN2, higher input voltage at 2.5 V to 5.5 V Range		6	A
		VIN1 or VIN2, higher input voltage at 1.5 V to 2.5 V Range		4	A
T_J	Maximum Junction Temperature			150	°C
T_{STG}	Storage Junction Temperature		- 65	150	°C
T_A	Ambient Operating Temperature Range		- 40	105	°C
θ_{JA}	Thermal Resistance, Junction to Ambient			60	°C/W
ESD	Electrostatic Discharge Capability	Human Body Model, JESD22-A114	± 2		kV
		Charged Device Model, JESD22-C101	± 2		

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Max.	Unit
V_{IN1}, V_{IN2}	Input Voltage	1.5	5.5	V
V_{S1}, V_{S2}	Control Pin Voltage	0	5.5	V

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ELECTRICAL CHARACTERISTICS

V_{IN1} = V_{IN2} = 1.5 V to 5.5 V and T_A = 25 °C. Unless otherwise noted

Symbol	Parameter	Conditions		Min	Typ	Max	Units
Basic Operation							
$I_{STBY_VIN1,2}$	VIN Unselect Channel Standby Current	V_{IN1} = 5.5 V, I_{OUT} = 0 mA, S2 = VIN1, S1 = 0 V, VOUT= VIN2 or V_{IN2} = 5.5 V, I_{OUT} = 0 mA, S1 = S2 = VIN2, VOUT = VIN1	T_A = 25 °C		1.2	2	µA
			T_A = 85 °C (1)		1.4		
			T_A = 105 °C (1)		1.6		
$I_{Q_VIN1,2}$	VIN Quiescent Current	V_{IN1} = 5.5 V, I_{OUT} = 0 mA, S1 = S2 = VIN1, VOUT = VIN1 or V_{IN2} = 5.5 V, I_{OUT} = 0 mA, S1 = VIN1, S2 = 0 V, VOUT = VIN2	T_A = 25 °C		1.4	2.2	
			T_A = 85 °C (1)		1.6		
			T_A = 105 °C (1)		2		
$I_{SD_VIN1,2}$	VIN Shutdown Current	$V_{IN1,2}$ = 5.5 V, V_{S2} = 0 V, V_{S1} = 5.5 V, V_{OUT} = High-Z	T_A = 25 °C		1	1.5	
			T_A = 85 °C (1)		2		
			T_A = 105 °C (1)		3.6		
I_{S1}, I_{S2}	S1 and S2 Pin Leakage	V_{S1} = V_{S2} = 5.5 V			2		nA
R_{ON}	On-Resistance	$V_{IN1,2}$ = 5.5 V, I_{OUT} = 200 mA	T_A = 25 °C		15	22	mΩ
			T_A = 85 °C (1)		18		
			T_A = 105 °C (1)		19		
		$V_{IN1,2}$ = 3.3 V, I_{OUT} = 200 mA	T_A = 25 °C		20	28	
			T_A = 85 °C (1)		24		
			T_A = 105 °C (1)		25		
		$V_{IN1,2}$ = 1.8 V, I_{OUT} = 200 mA	T_A = 25 °C		36	44	
			T_A = 85 °C (1)		43		
			T_A = 105 °C (1)		45		
		$V_{IN1,2}$ = 1.5 V, I_{OUT} = 200 mA	T_A = 25 °C		48	55	
			T_A = 85 °C (1)		56		
			T_A = 105 °C (1)		58		
V_{TH}	S1 Pin Threshold Voltage	$V_{IN1,2}$ = 1.5 V to 5.5 V		1.05	1.2	1.35	V
		Hysteresis			230		mV
V_{IH}	S2 Input Logic High Voltage	$V_{IN1,2}$ = 1.5 V to 5.5 V		1.2			V
V_{IL}	S2 Input Logic Low Voltage	$V_{IN1,2}$ = 1.5 V to 5.5 V				0.3	
TSD	Thermal Shutdown Protection Threshold (1)				140		°C
	Thermal Shutdown Release Hysteresis (1)				20		°C
Reverse Current Blocking Protection, GLF4012 Only							
V_{RCB_TH}	RCB Protection Threshold	$V_{IN1,2}$ = 3.3 V, VOUT – VIN		0	16	50	mV
V_{RCB_RL}	RCB Protection Release	$V_{IN1,2}$ = 3.3 V, VIN - VOUT		0	18	50	mV
t_{RCB}	RCB Response Time (1)	V_{OUT} > Selected VIN + 1 V			23		µs
I_{RCB}	RCB activation current (1)				0.7		A
Switching Characteristics							
V_{TR}	Auto Input Selection Trigger (1)	V_{INX} - V_{INY}, In automatic selection mode			230	300	mV
t_{SW}	Switching Over time In Manual Mode (1)	VIN1 to VIN2	V_{IN1} = 3.3 V, V_{IN2} = 5.5 V, C_{OUT} = 10 µF, R_L = 10 Ω		36		µs
		VIN2 to VIN1			18		

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ELECTRICAL CHARACTERISTICS (CONTINUED)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
t_{dON}	Turn-On Delay time (1)	$V_{IN1,2}$ = 5 V	C_{OUT} = 10 µF, R_L = 150 Ω		370		µs
		$V_{IN1,2}$ = 4.2 V			320		
		$V_{IN1,2}$ = 3.3 V			270		
		$V_{IN1,2}$ = 1.5 V			190		
t_R	VOUT Rise Time (1)	$V_{IN1,2}$ = 5 V			290		
		$V_{IN1,2}$ = 4.2 V			290		
		$V_{IN1,2}$ = 3.3 V			300		
		$V_{IN1,2}$ = 1.5 V			330		
t_{dOFF}	VOUT Turn-Off Delay Time (1)	$V_{IN1,2}$ = 5 V			60		
		$V_{IN1,2}$ = 4.2 V			70		
		$V_{IN1,2}$ = 3.3 V			70		
		$V_{IN1,2}$ = 1.5 V			100		
t_F	VOUT Fall Time (1)	$V_{IN1,2}$ = 5 V			2.5		ms
		$V_{IN1,2}$ = 4.2 V			2.5		
		$V_{IN1,2}$ = 3.3 V			2.4		
		$V_{IN1,2}$ = 1.5 V			3.4		

Note: 1. By design; characterized, not production tested.

APPLICATION DIAGRAM

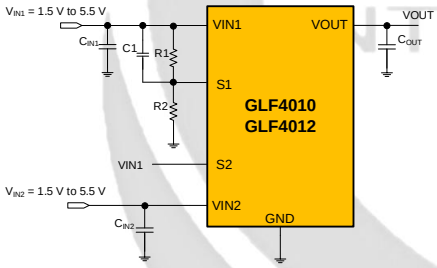

Figure 3. VIN1 Preference Selection Mode

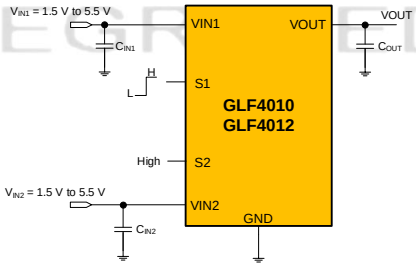

Figure 4. Manual Selection Mode by GPIO

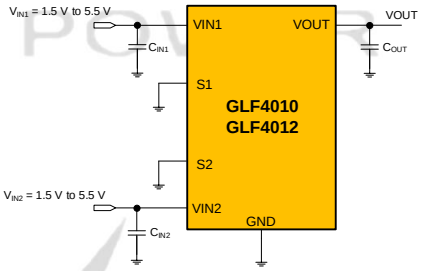

Figure 5. Auto Selection Mode

TRUTH TABLE AND TIMING DIAGRAM

Mode	S2	S1	Function
Manual (1)	High	> V_{TH}	VIN1 is selected
	High	< V_{TH}	VIN2 is selected
	Low	> V_{TH}	Both channels are off
Auto (1), (2)	Low	< V_{TH}	Auto-Input selection
VIN1 Preference (1)	High	> V_{TH} (Divided by external resistor)	VIN1 is selected
	High	< V_{TH} (Divided by external resistor)	VIN2 is selected

Note : (1) V_{INX} or V_{INY} > 1.5 V (V_{IN_MIN}), High = V_{S2} > V_{IH}, Low = V_{S2} < V_{IL}
(2) It is recommended to use the auto mode when V_{INX} - V_{INY} ≥ 500 mV.

Table 1. Truth Table of Input Source Selection

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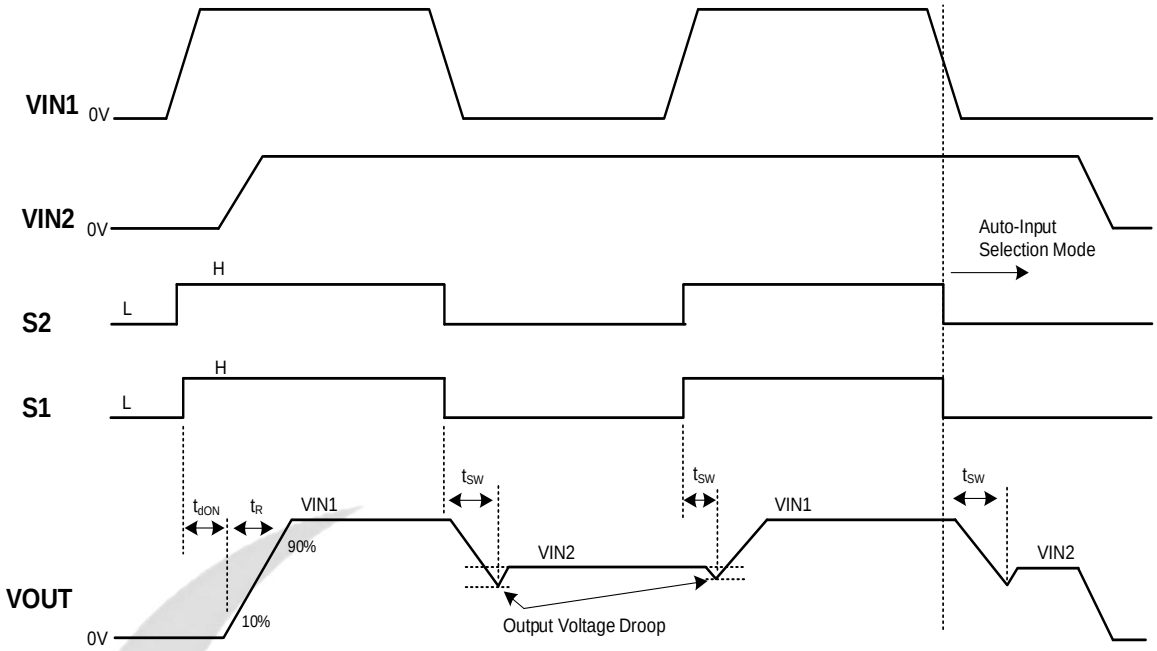

Figure 6. Timing Diagram, VIN1 Preference Mode (Figure 3) with S2 tied to VIN1
High : V_{S2}, V_{S1} > V_{TH}, Low : V_{S2}, V_{S1} < V_{TH}

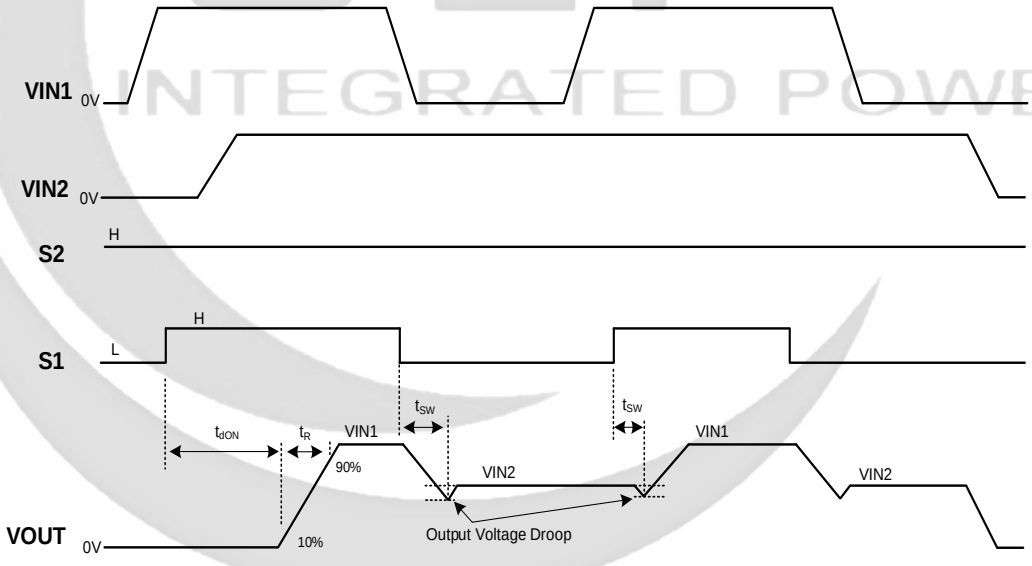

Figure 7. Timing Diagram, Manual Mode (Figure 4) with S1 controlled by GPIO
High: V_{S2} > V_{IH}, V_{S1} > V_{TH}, Low: V_{S2} < V_{IL}, V_{S1} < V_{TH}

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TYPICAL PERFORMANCE CHARACTERISTICS

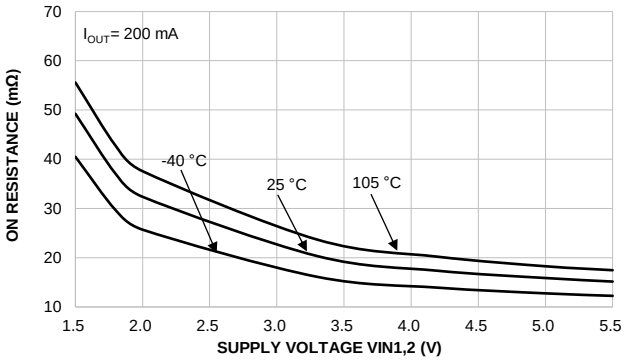

Figure 8. On-Resistance vs. Supply Voltage

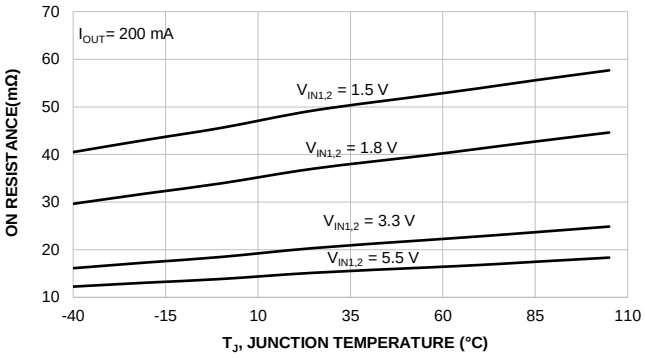

Figure 9. On-Resistance vs. Temperature

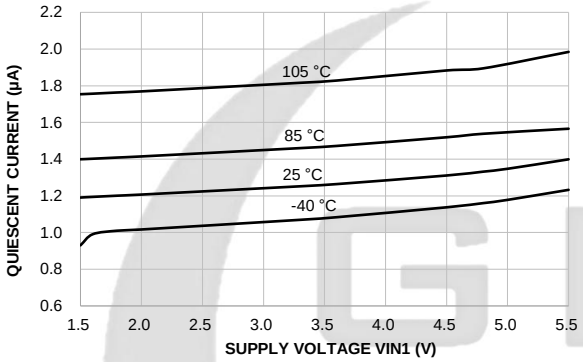

Figure 10. VIN1 Quiescent Current vs. Supply Voltage

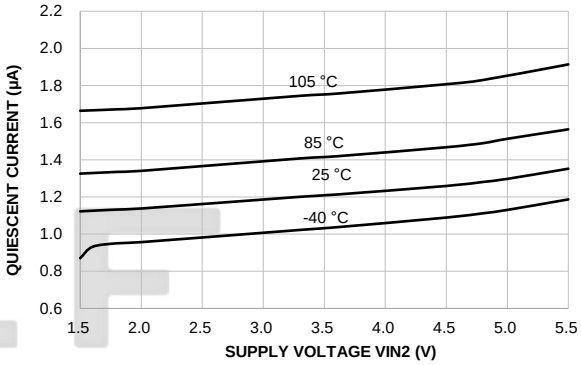

Figure 11. VIN2 Quiescent Current vs. Supply Voltage

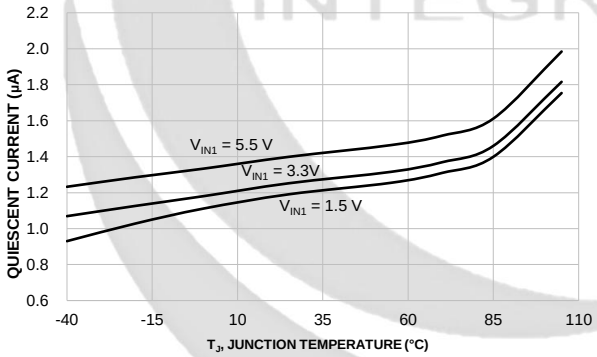

Figure 12. VIN1 Quiescent Current vs. Temperature

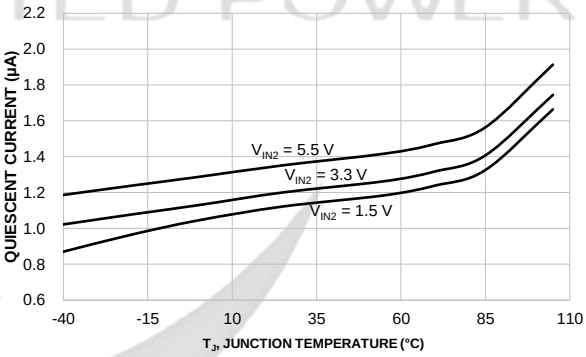

Figure 13. VIN2 Quiescent Current vs. Temperature

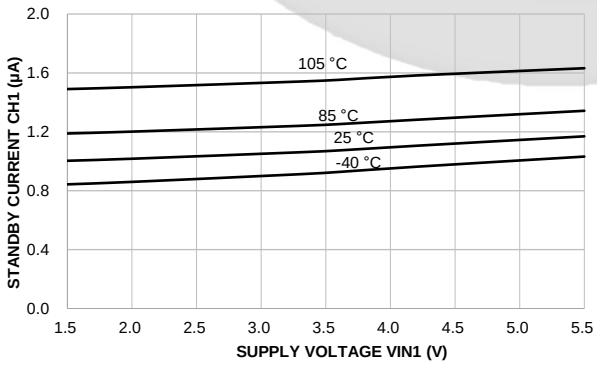

Figure 14. VIN1 Standby Current vs. Supply Voltage

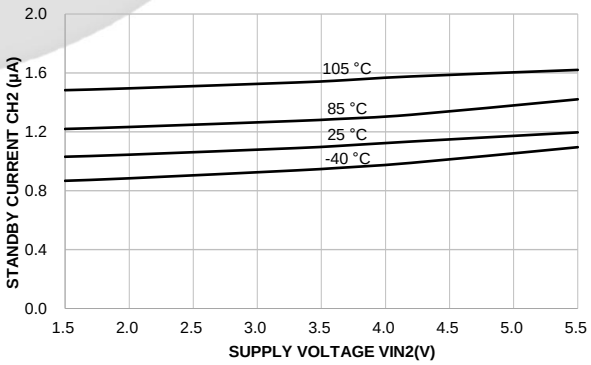

Figure 15. VIN2 Standby Current vs. Supply Voltage

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TYPICAL PERFORMANCE CHARACTERISTICS (CONTINUED)

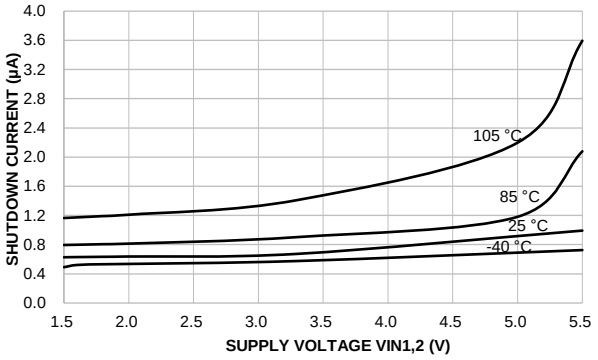

Figure 16. VIN Shutdown Current vs. Supply Voltage

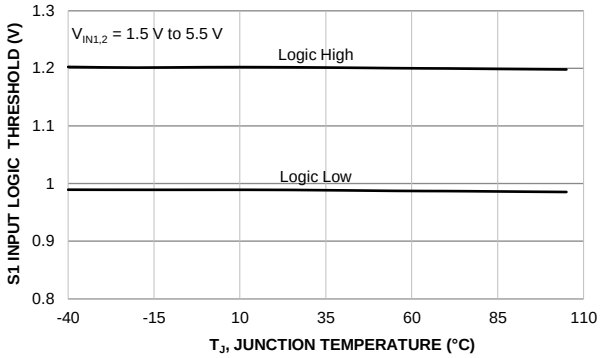

Figure 17. S1 Input Logic Threshold vs. Temperature

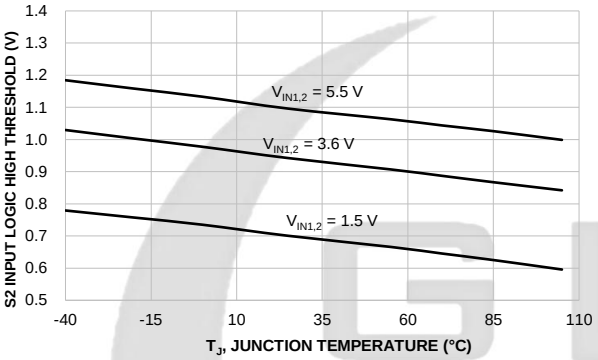

Figure 18. S2 Input Logic High Threshold vs. Temperature

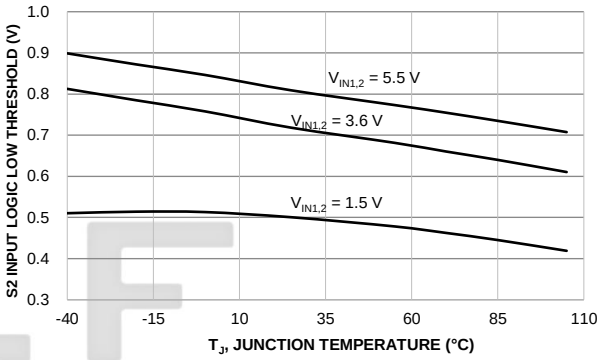

Figure 19. S2 Input Logic Low Threshold vs. Temperature

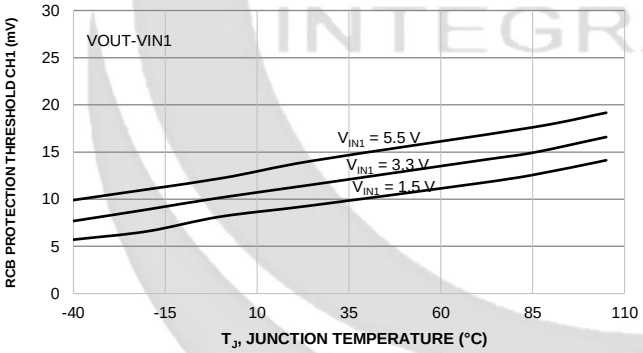

Figure 20. GLF4012 CH1 RCB Protection Threshold vs. Temperature

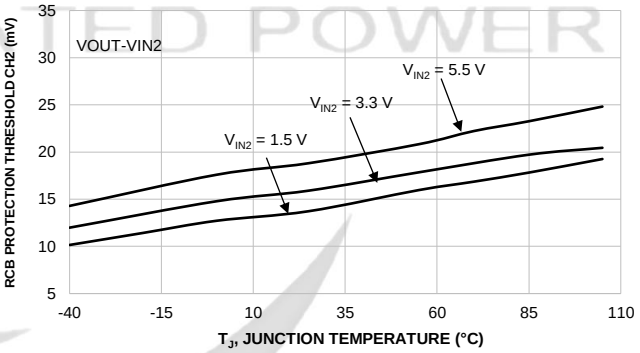

Figure 21. GLF4012 CH2 RCB Protection Threshold vs. Temperature

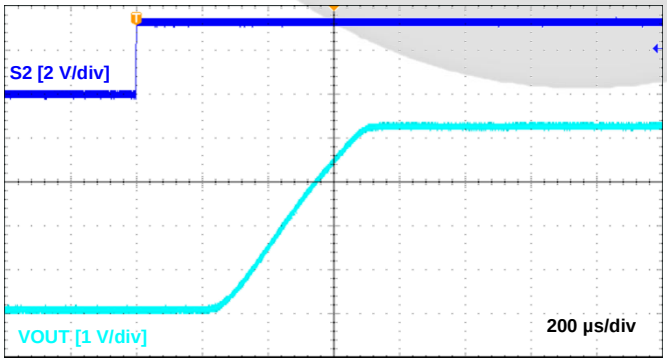

Figure 22. Turn-On Response, CH1
V_{IN1}=4.2 V, C_{IN}=C_{OUT} =10 µF, R_L=100 Ω

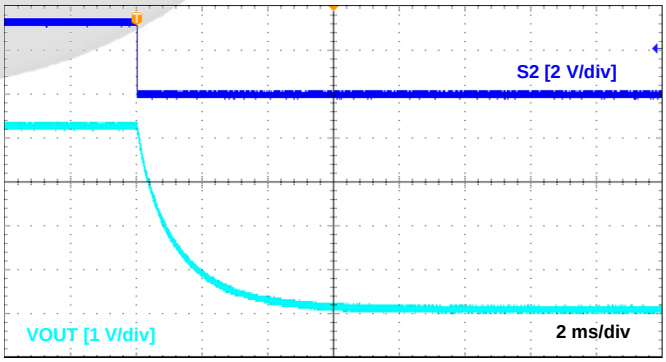

Figure 23. Turn-Off Response, CH1
V_{IN1}=4.2 V, C_{IN}=C_{OUT} =10 µF, R_L=100 Ω

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TYPICAL PERFORMANCE CHARACTERISTICS (CONTINUED)

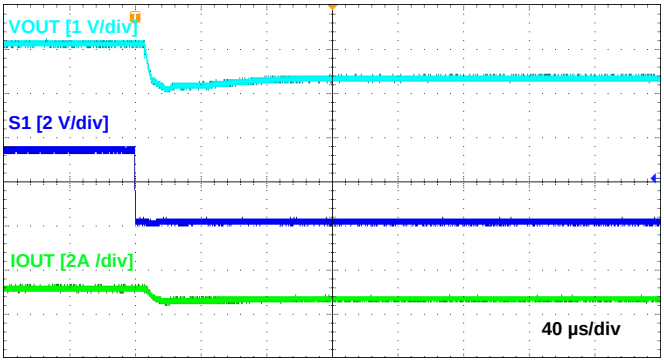


Figure 24. VOUT Switchover from 5.0 V to 4.2 V
V_{IN1}=5.0 V, V_{IN2}=4.2 V, C_{OUT}=47 µF, R_L=1.5 Ω
S2=3.3 V, S1 controlled by GPIO

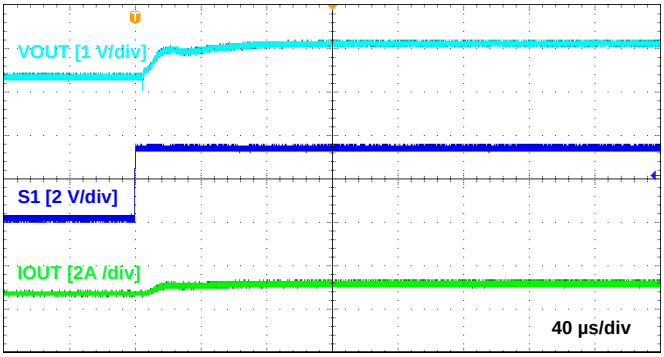
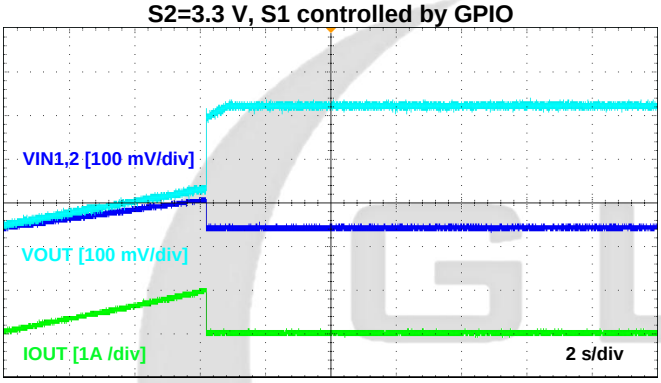


Figure 25. VOUT Switchover from 4.2 V to 5.0 V
V_{IN1}=5.0 V, V_{IN2}=4.2 V, C_{OUT}=47 µF, R_L=1.5 Ω
S2=3.3 V, S1 controlled by GPIO



Fiqure 26. Reverse Current Blocking on Each Channel
$V_{IN1,2}$=3.3 V, V_{OUT}=3 V to 3.4 V, C_{IN}=C_{OUT}=10 µF

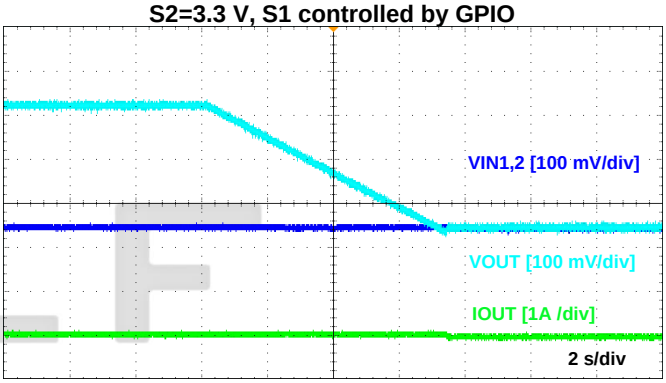


Figure 27. Reverse Current Blocking Release
$V_{IN1,2}$=3.3 V, V_{OUT}=3.4 V to 3 V, C_{IN}=C_{OUT}= 10 µF

APPLICATION INFORMATION

The GLF4010 and GLF4012 are fully integrated power mux IC with the input voltage range from 1.5 V to 5.5 V. It has symmetrical two channels and a fixed slew rate control to limit the inrush current during turn on. It also has very low on-resistance to reduce conduction loss. In the off state, it consumes very low leakage current to avoid unwanted standby current and save input power supply.

Input Source Selection

According to the state of S2 and S1 pins, the GLF4010 and GLF4012 offer the automatic, manual selection mode and VIN1 preference mode. In each mode, the VOUT connects to one input source. Do not leave both S2 and S1 pins floating.

Mode	S2	S1	Function
Manual	High	> V_{TH}	VIN1 is selected
	High	< V_{TH}	VIN2 is selected
	Low	> V_{TH}	Both channels are off
Auto	Low	< V_{TH}	Auto-Input selection
VIN1 Preference	High	> V_{TH} (Divided by external resistor)	VIN1 is selected
	High	< V_{TH} (Divided by external resistor)	VIN2 is selected

Table 2. Input Source Selection

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In VIN1 preference mode (refer to Figure 3), the S2 pin is connected to VIN1. The S1 pin is connected to the midpoint of a voltage divider formed by two resistors. The voltage at the S1 pin determines the operating state of the GLF4010 and GLF4012. When VIN1 is applied and the voltage at the S1 pin is higher than the threshold voltage (V_{TH}), the VOUT is powered by VIN1. As VIN1 voltage drops, if the voltage at the S1 pin falls below V_{TH}, VOUT automatically switches over to VIN2.

For applications, where a General-Purpose Input/Output (GPIO) pin is used to select the input source (refer to Figure 4), the GPIO pin connects directly to the S1 pin, and the S2 pin is set high. When the GPIO pin is high, VIN1 is selected as the input. Conversely, when the GPIO pin is low, VIN2 is selected.

For applications, if both S1 & S2 are low (refer to Figure 5), the GLF4010 and GLF4012 will choose a higher input voltage source to VOUT automatically. It is recommended to use V_{INX} - V_{INY} ≥ 500 mV for the auto mode, which will effectively prevent a series of problems caused by parasitic resistance in wires or PCB when the load current is high.

Design Example for Switching-Over Trigger Voltage Calculation:

Parameter	Value
VIN1	4.5 V
VIN2	1 cell Lithium Thionyl Chloride Battery
Selection Mode	VIN1 Preference Selection

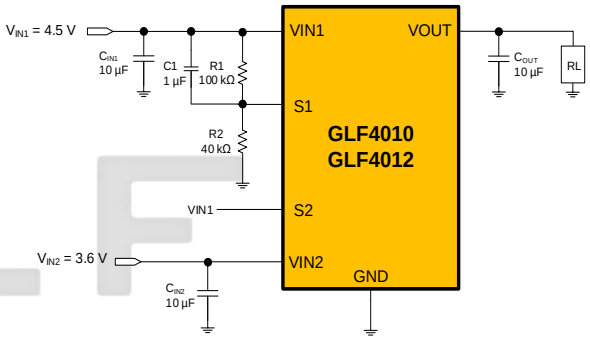

Figure 28. Design Example for V_{SW_TRG} Calculation

The value of the switching-over trigger voltage is determined by the following equation.

$$V_{SW_TRG} = V_{TH} \times (1 + R1 / R2)$$

Where, V_{SW_TRG}: Switching-over trigger voltage when VIN1 is unplugged.

V_{TH}: S1 pin threshold voltage

For downstream systems requiring power supply switching with minimal output voltage drop, the GL4010 and GLF4012 can reduce the voltage drop during transition from the primary input (VIN1) to the secondary input (VIN2) upon removal of VIN1. In this example, the switching trigger voltage is set to 3.5 V (when 4.5 V is removed) using resistors R1 (100 kΩ) and R2 (40 kΩ).

Output Voltage Droop at Switching Over

During switching events, the droop in output voltage is influenced by both the load current and the output capacitance. A higher load current at the switching point will result in a larger voltage droop. To reduce this droop when a large load current is required during the transition, it is recommended to use a large output capacitor. The Figure 29 shows the output voltage droop characteristics. A reminder: the minimum output voltage droop point will also be affected by the load transient capability of the input power supply.

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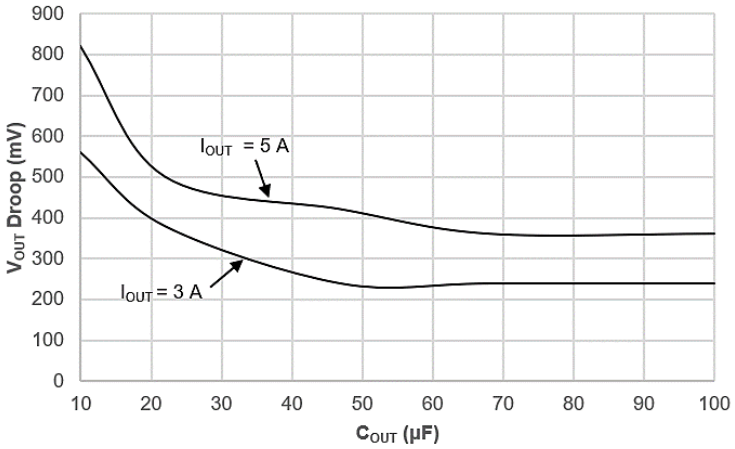

Figure 29. Output Voltage Droop at Switching Over from VIN1 (5.0 V) to VIN2 (3.3 V), Manual mode

Thermal Shutdown Protection

The GLF4010 and GLF4012 have a thermal shutdown protection. When the junction temperature exceeds TSD threshold, the device will turn off the internal main switch to protect itself from damage due to overheating. When the junction temperature drops below the TSD hysteresis, the device will return to normal operation.

Reverse Current Blocking

The GLF4012 has reverse current blocking protection. The reverse current blocking protection triggers when the output voltage rises above an input voltage plus the reverse current blocking threshold (V_{RCB_TH}). The main FET immediately shuts off to prevent reverse current flow. It's important to note that some reverse current might exist before V_{RCB_TH} is reached. Normal operation resumes when the output voltage falls below the input minus the reverse current blocking release voltage (V_{RCB_RL}). An additional clamping component and a high output capacitance are recommended to safeguard against potential damage from high output voltage spikes.

Board Layout

All the external components should be placed to GLF4010 and GLF4012 as close as possible. All traces should be as short as possible to minimize parasitic inductance. Wide traces of VIN, VOUT and GND can reduce parasitic effects under dynamic operations to improve thermal performance at high current loading.

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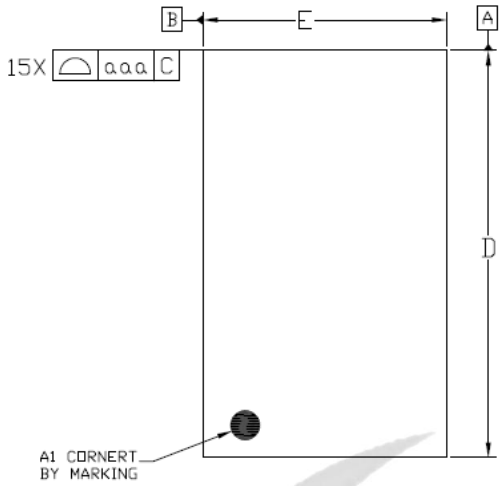
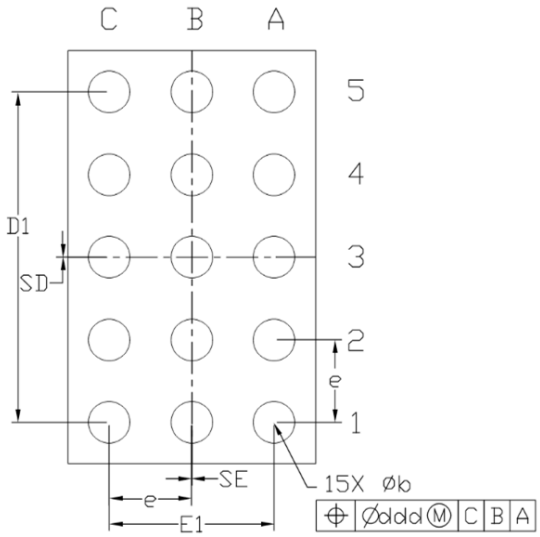
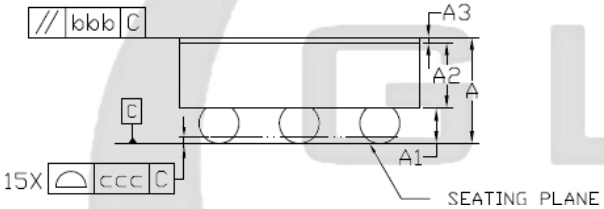
PACKAGE OUTLINE



TOP VIEW

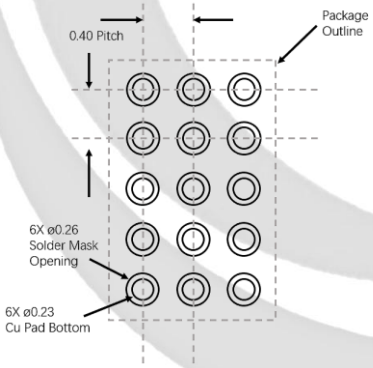


BOTTOM VIEW



REF.	Dimensions Ref.		
	Min.	Nom.	Max.
A	0.500	0.550	0.600
A1	0.149	0.175	0.201
A2	0.325	0.350	0.375
A3	0.020	0.025	0.030
D	1.955	1.970	1.985
E	1.155	1.170	1.185
D1	1.550	1.600	1.650
E1	0.750	0.800	0.850
b	0.197	0.232	0.267
e	0.400 BSC		
SD	0.000 BSC		
SE	0.000 BSC		
Tol. of Form & Position			
aaa	0.10		
bbb	0.10		
ccc	0.05		
ddd	0.05		

Recommended Footprint



PACKAGING INFORMATION

Part Number	Package	Pins	Top Mark	Moisture Sensitivity Level	Environmental Information
GLF4010-SA7	WLCSP	15	IA	MSL1	ROHS+HF
GLF4012-SA7	WLCSP	15	IC	MSL1	ROHS+HF

Notes

1. ALL DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGRESS)
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.
3. A3: BACKSIDE LAMINATION

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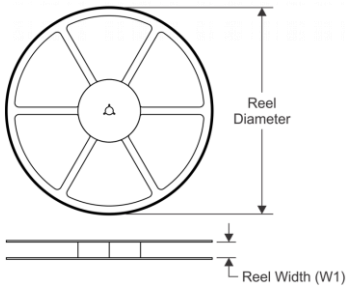
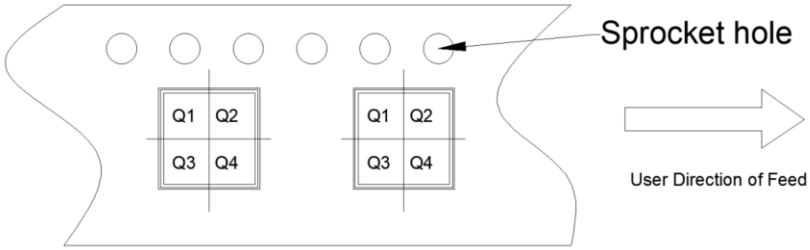
TAPE AND REEL INFORMATION

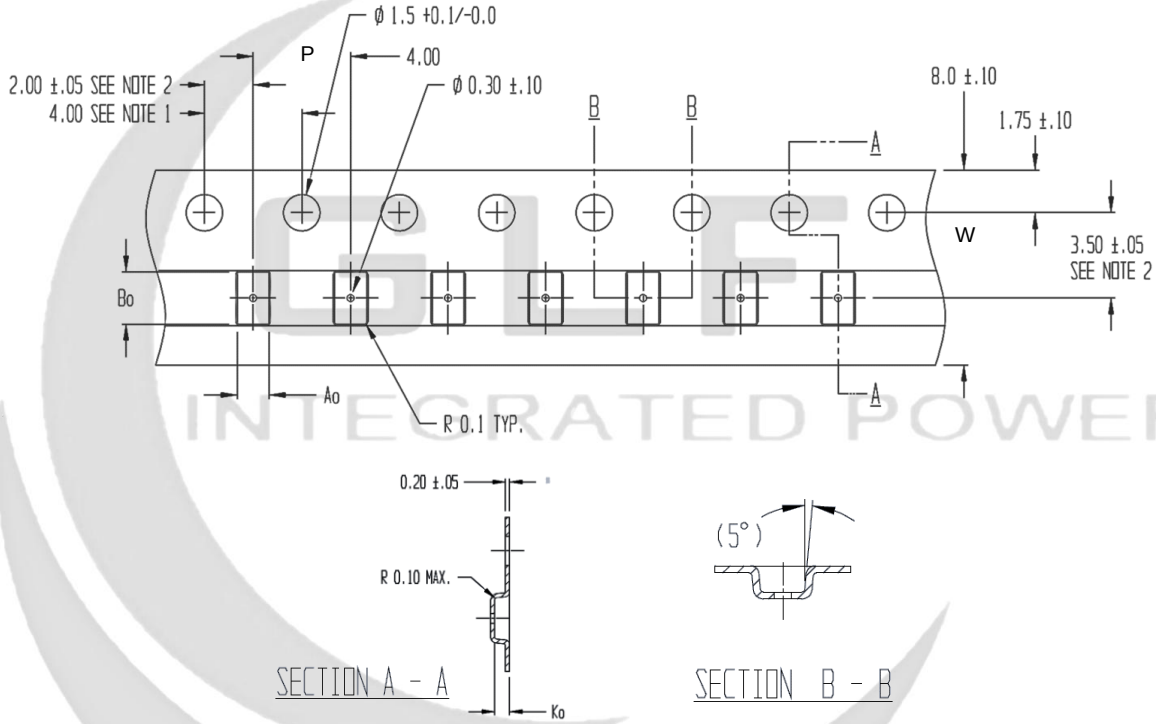
REEL DIMENSIONS



QUADRANT ASSIGNMENTS PIN 1 ORIENTATION TAPE



TAPE DIMENSIONS



Device	Package	Pins	SPQ	Reel Diameter (mm)	Reel Width W1	A0	B0	K0	P	W	Pin1
GLF4010-SA7	WLCSP	15	3000	180	9	1.32	2.15	0.77	4	8	Q2
GLF4012-SA7	WLCSP	15	3000	180	9	1.32	2.15	0.77	4	8	Q2

Remark:

A0: Dimension designed to accommodate the component width

B0: Dimension designed to accommodate the component length

K0: Dimension designed to accommodate the component thickness

W: Overall width of the carrier tape

P: Pitch between successive cavity centers

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SPECIFICATION DEFINITIONS

Document Type	Meaning	Product Status
Target Specification	This is a target specification intended to support exploration and discussion of critical needs for a proposed or target device. Parameters including the typical, minimum, and maximum values are desired, or target. GLF reserves the right to change contents at any time without warning or notification. A target specification will not guarantee the future production of the device.	Design / Development
Preliminary Specification	This is a draft version of a product specification which is under internal review and subject to change. GLF reserves the right to change the specification at any time without warning or notification. A preliminary specification will not guarantee the future production of the device.	Qualification
Product Specification	This document represents the characteristics of the device.	Production

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